FIG.1 PRIOR ART

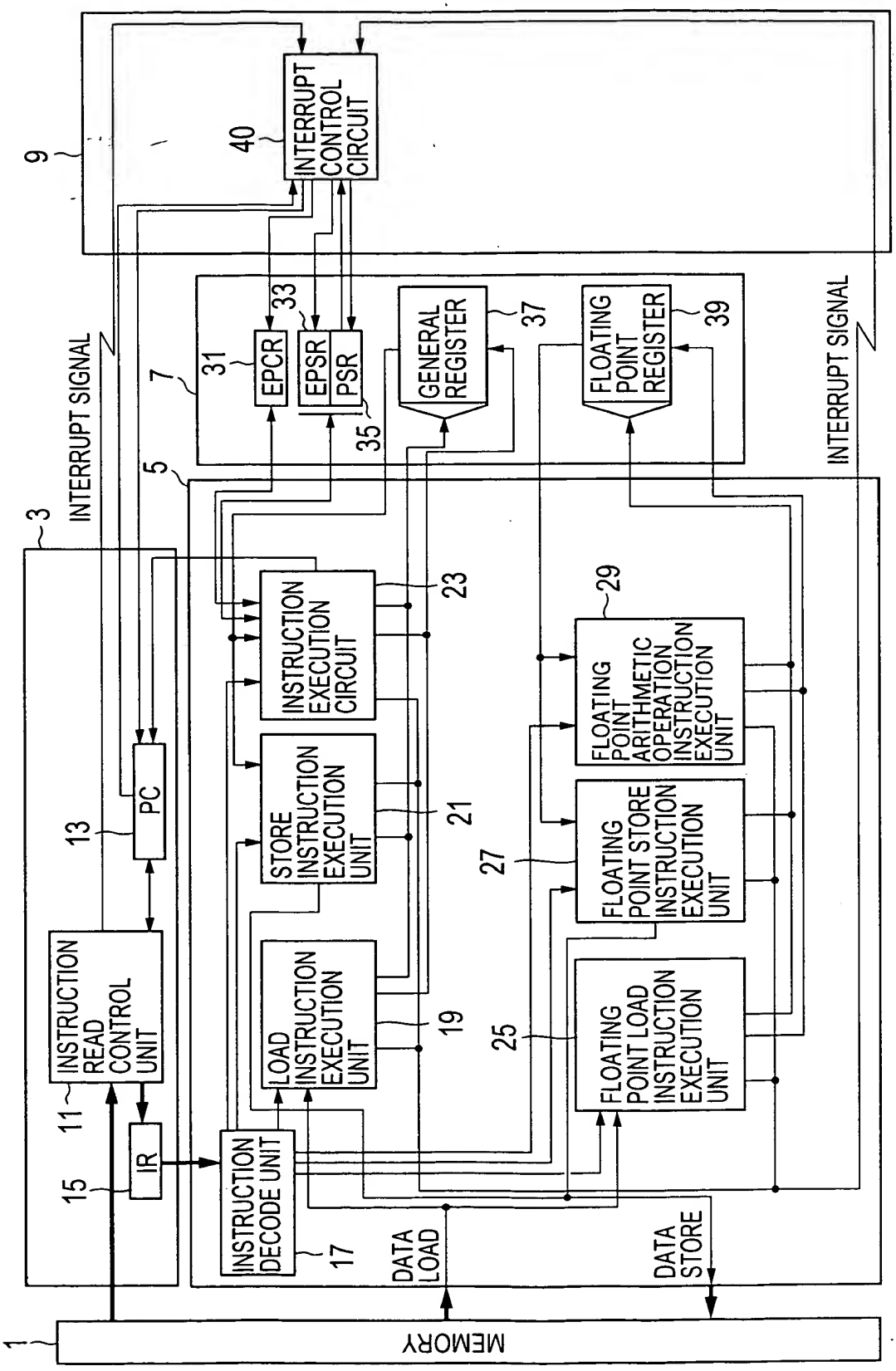

FIG. 2 PRIOR ART

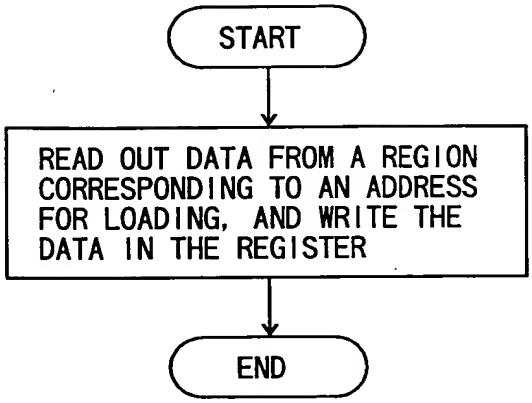

FIG. 3 PRIOR ART

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FIG. 4 PRIOR ART

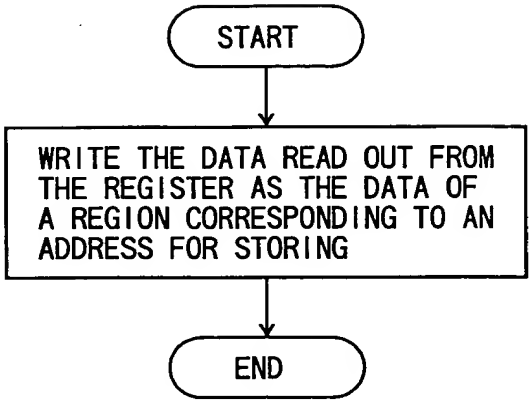

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FIG. 5 PRIOR ART

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FIG.6 PRIOR ART

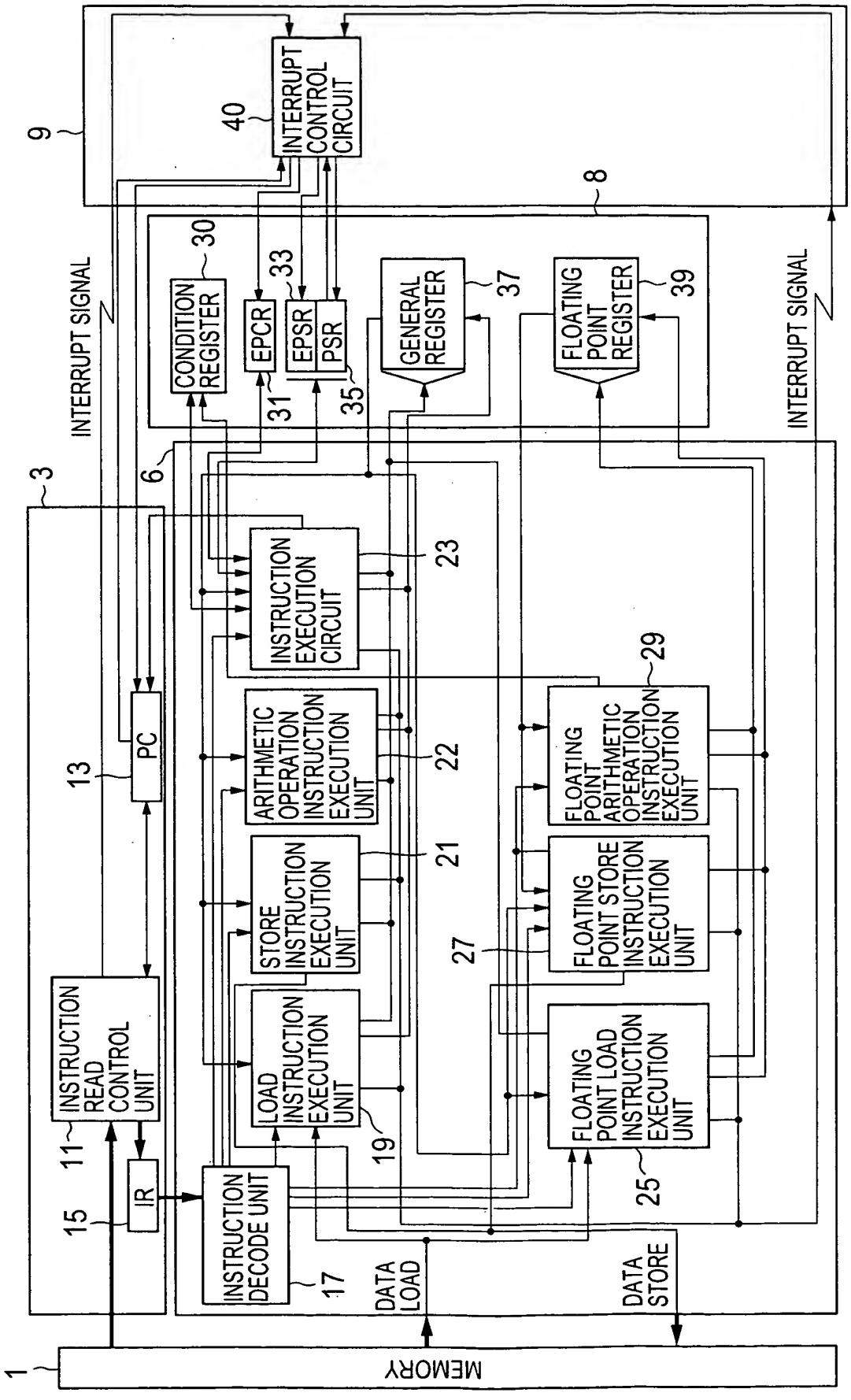

FIG. 7 PRIOR ART

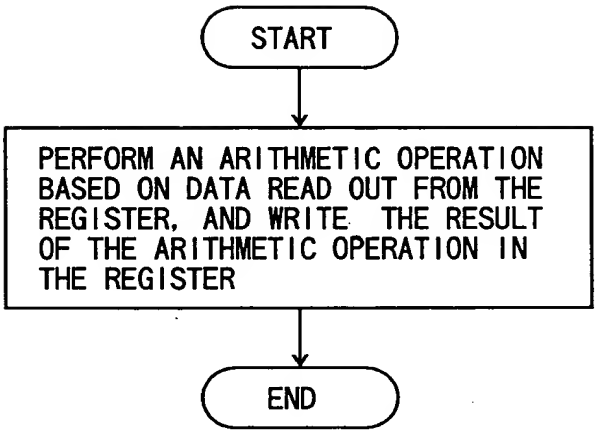

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FIG.8 PRIOR ART

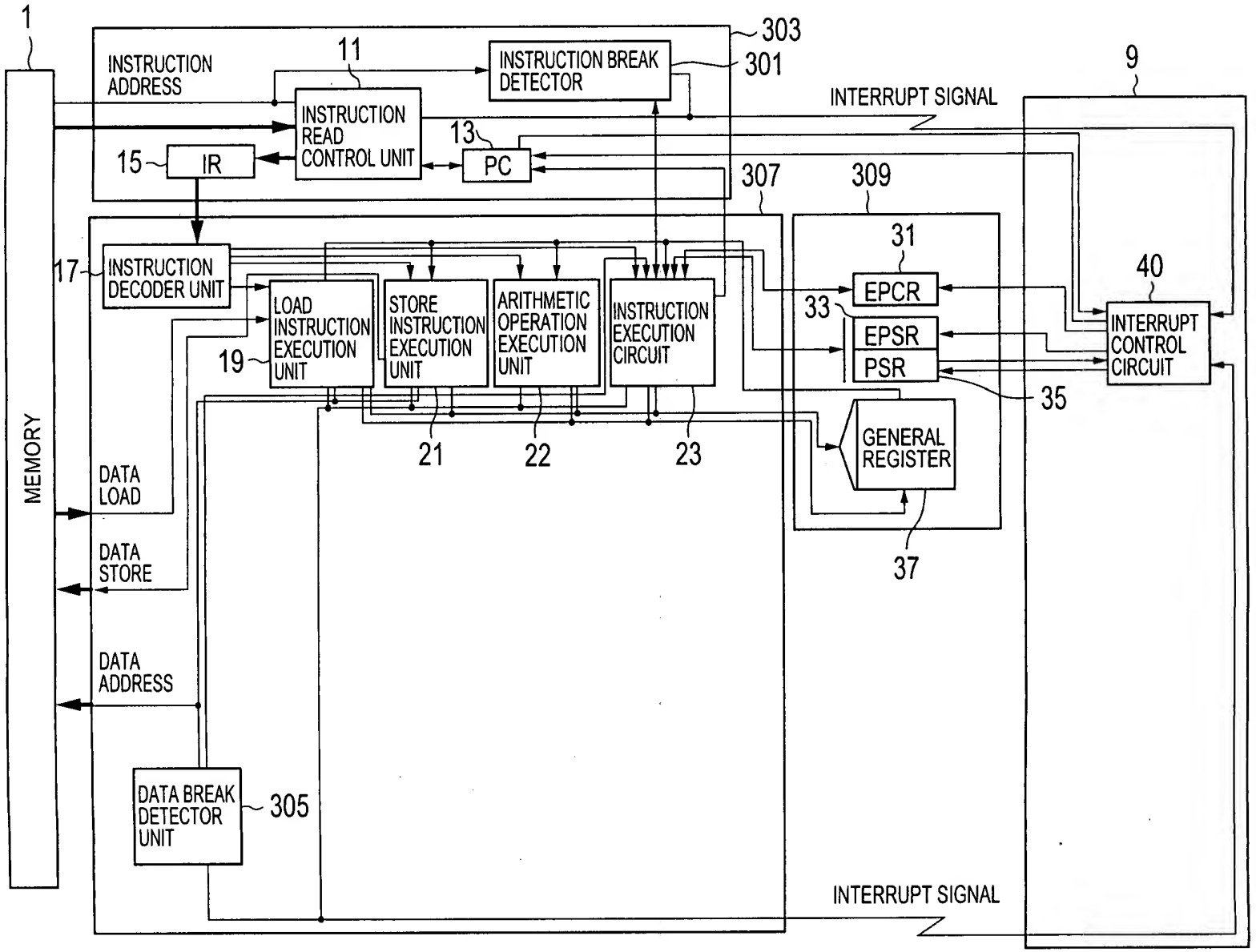

FIG.9 PRIOR ART

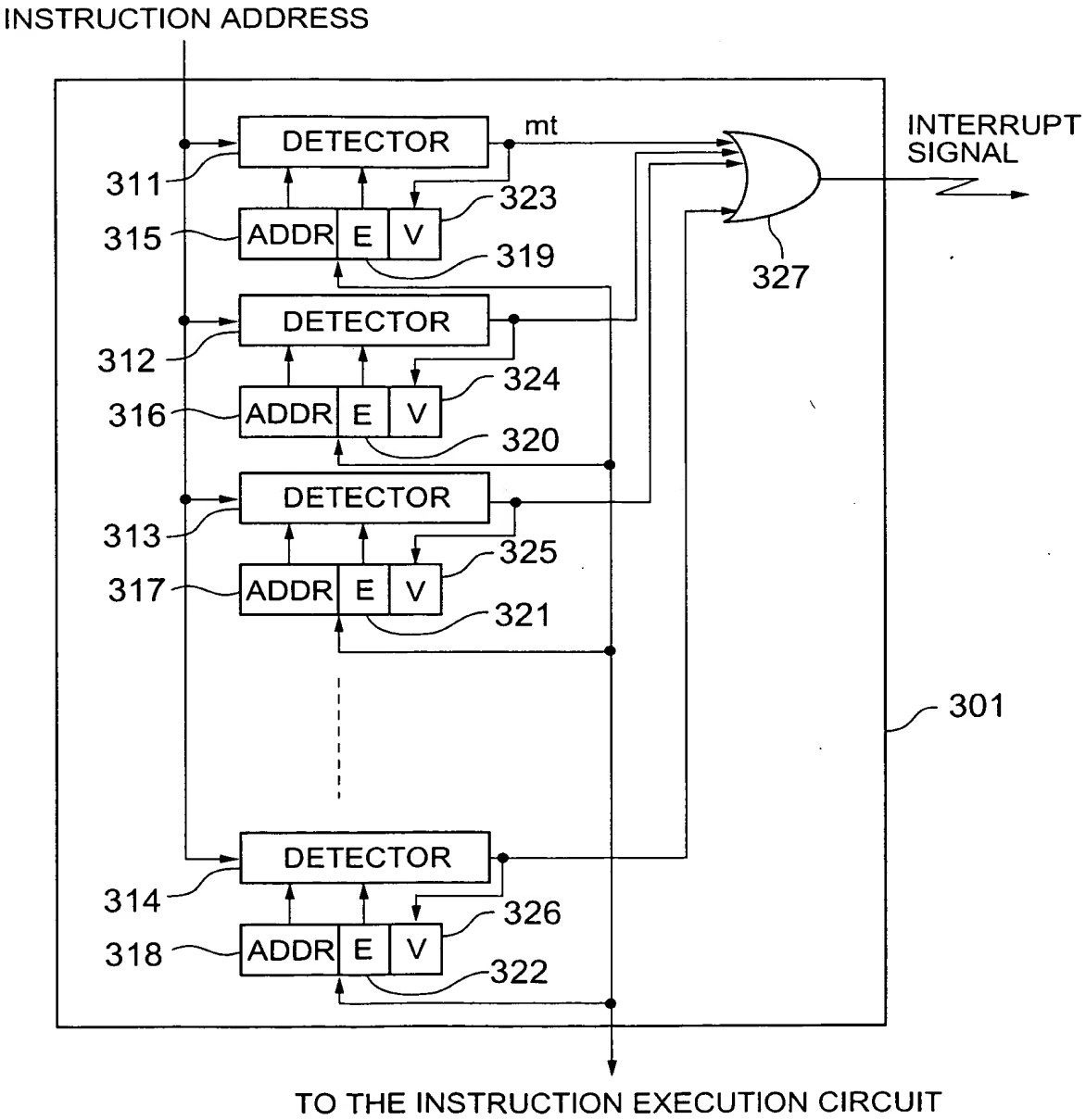

FIG.10 PRIOR ART

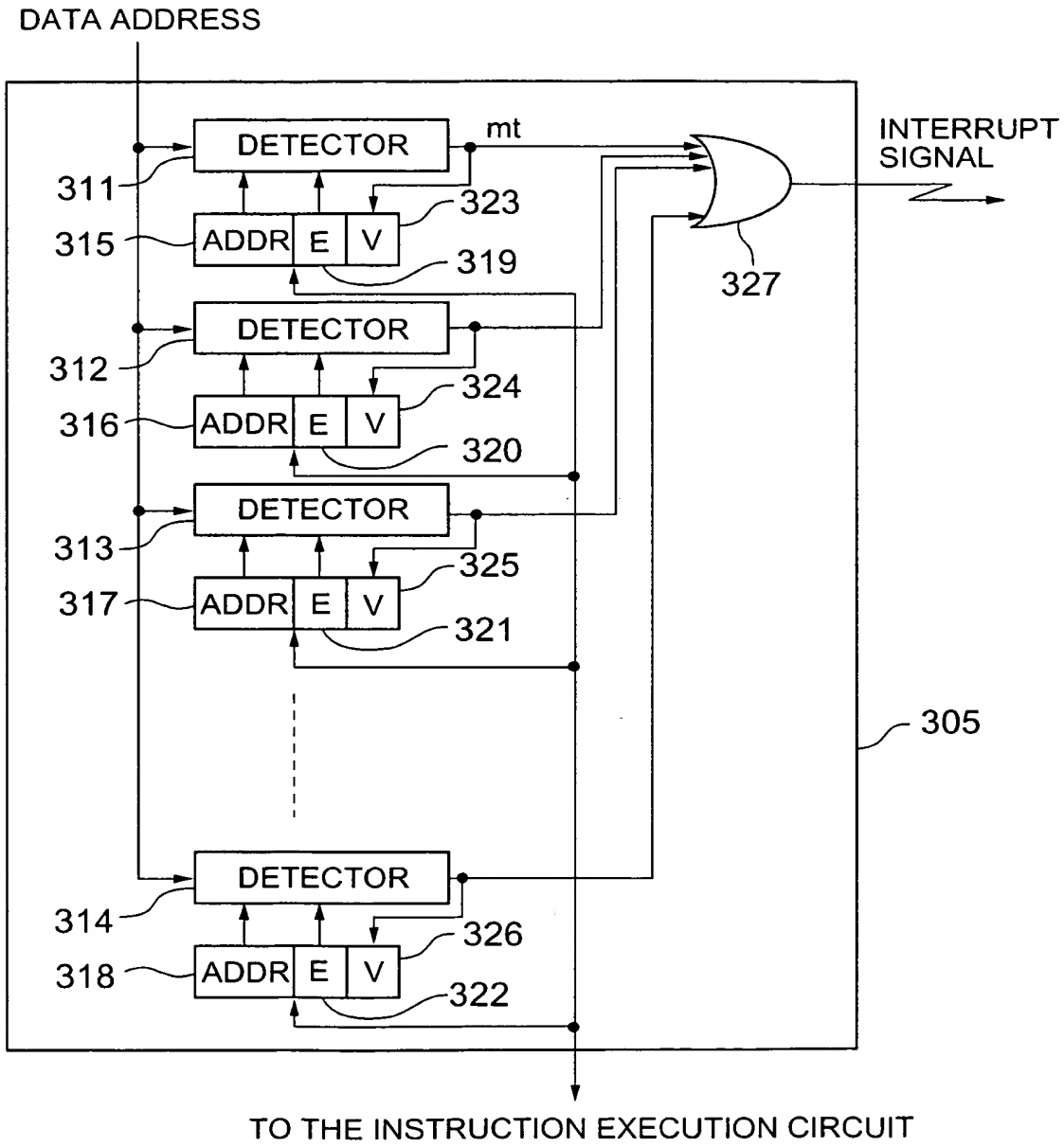

FIG.11 PRIOR ART

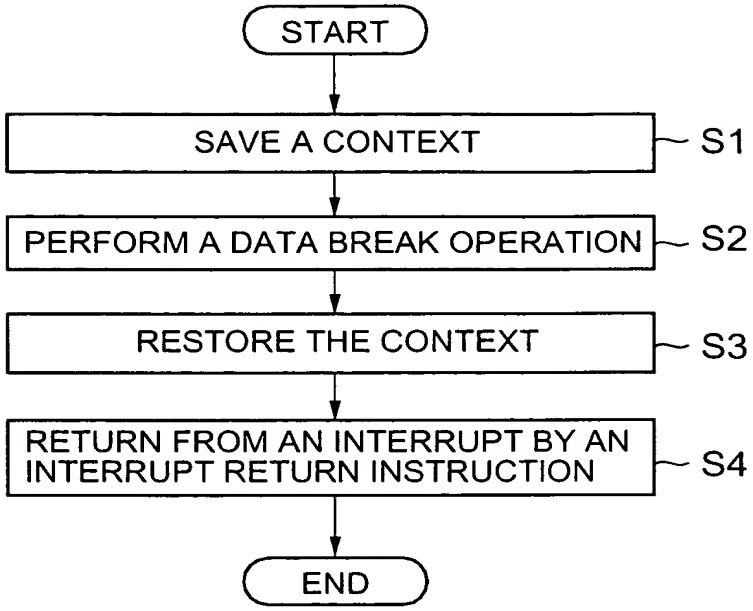

FIG.12 PRIOR ART

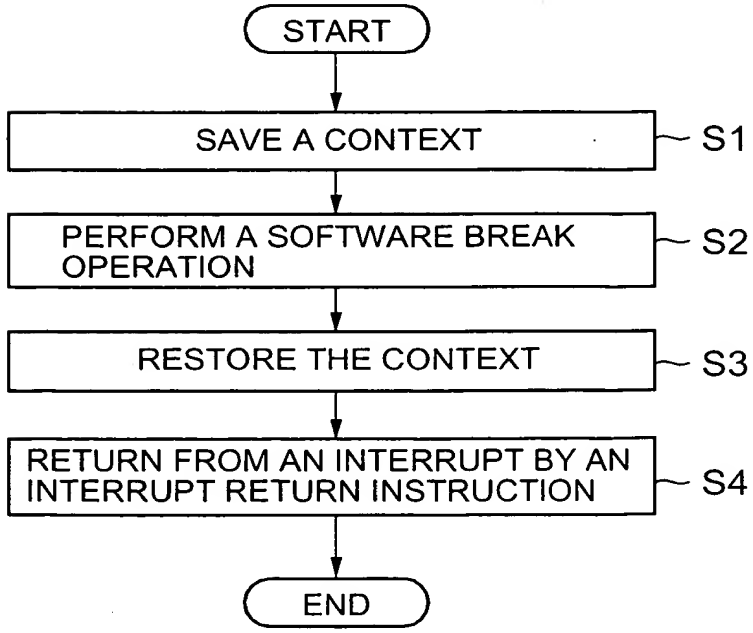

FIG.13

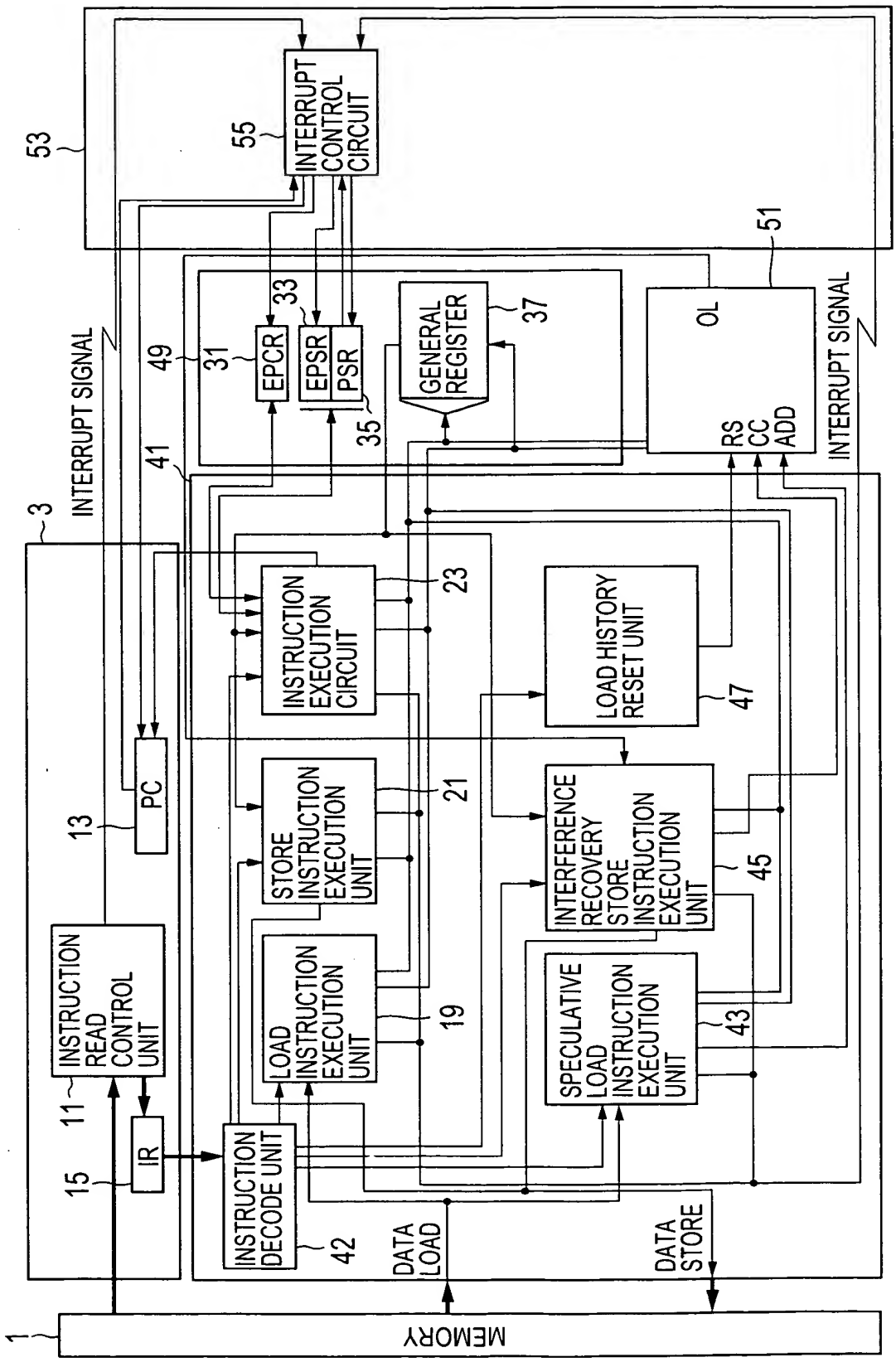
MEMORY
1
3
INTERRUPT SIGNAL
INTERRUPT SIGNAL
53
55
INTERRUPT CONTROL CIRCUIT
51
OL
RS
CC
ADD
49
31
EPCR
33
EPSR
PSR
35
GENERAL REGISTER
37
41
PC
13
INSTRUCTION READ CONTROL UNIT
11
IR
15
INSTRUCTION DECODE UNIT
42
INSTRUCTION EXECUTION CIRCUIT
23
LOAD HISTORY RESET UNIT
47
STORE INSTRUCTION EXECUTION UNIT
21
INTERFERENCE RECOVERY STORE INSTRUCTION EXECUTION UNIT
45
LOAD INSTRUCTION EXECUTION UNIT
19
SPECULATIVE LOAD INSTRUCTION EXECUTION UNIT
43
DATA LOAD
DATA STORE

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FIG.14

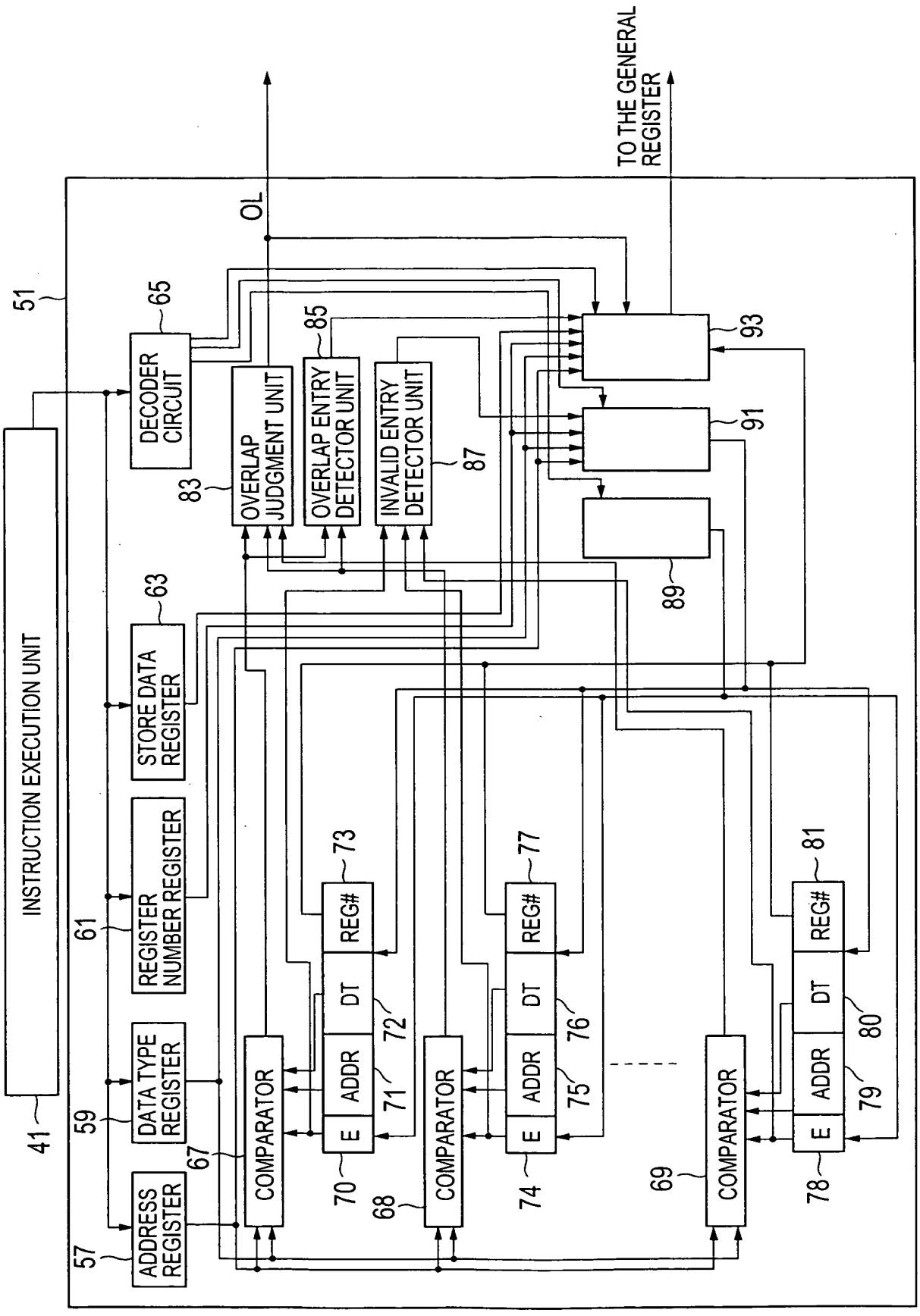


FIG. 15

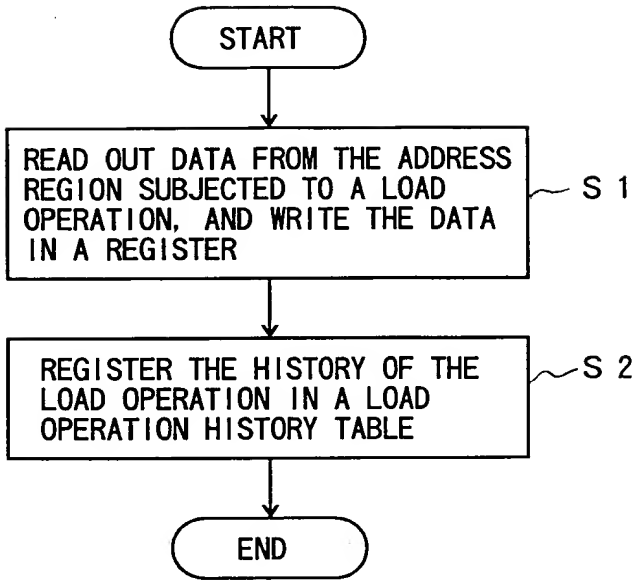
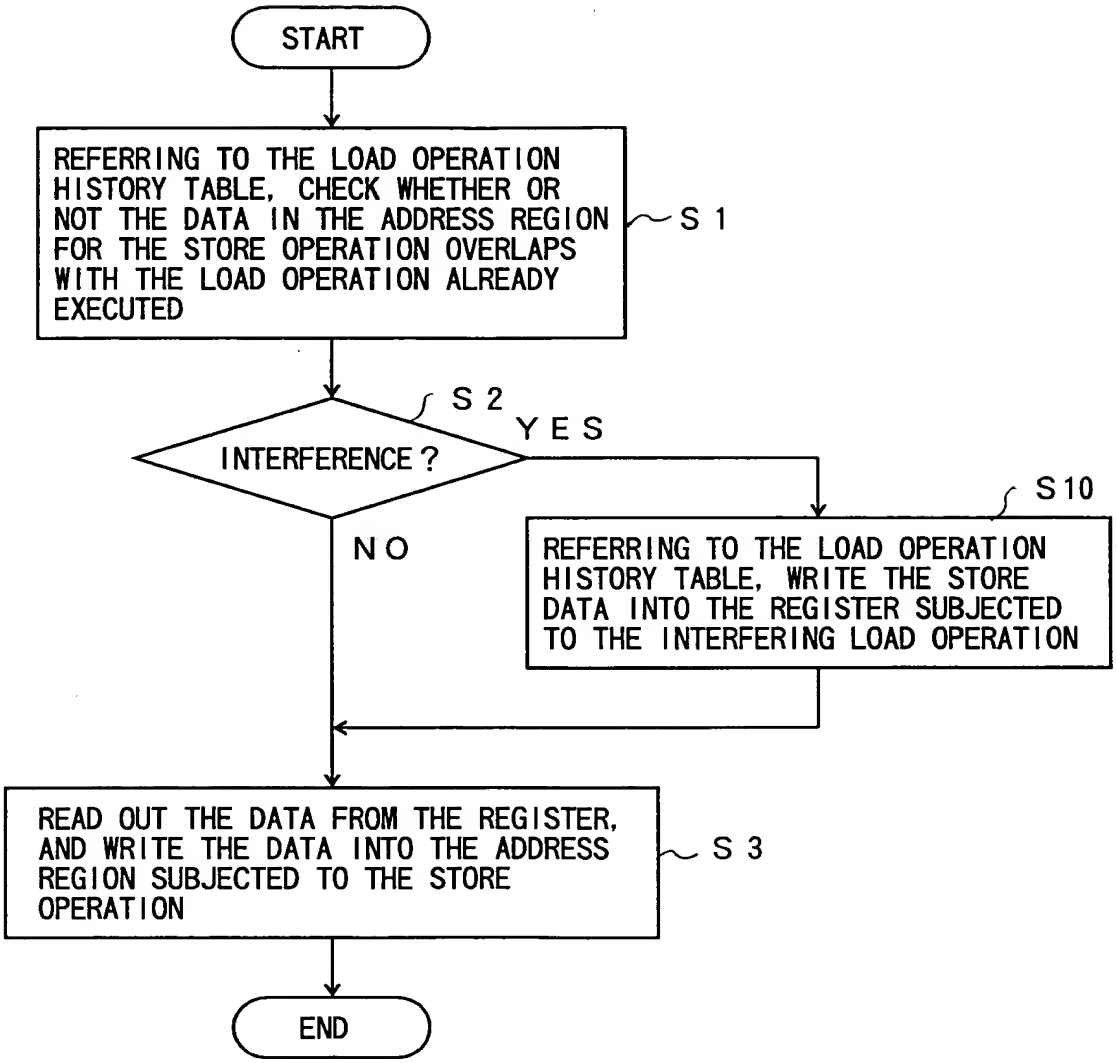

START
READ OUT DATA FROM THE ADDRESS REGION SUBJECTED TO A LOAD OPERATION, AND WRITE THE DATA IN A REGISTER
S 1
REGISTER THE HISTORY OF THE LOAD OPERATION IN A LOAD OPERATION HISTORY TABLE
S 2
END

FIG. 16

FIG. 17



0353541.1250

0 5 4 5 0 4 5 0 5 5 0 5 5 0

FIG. 18

FIG. 19

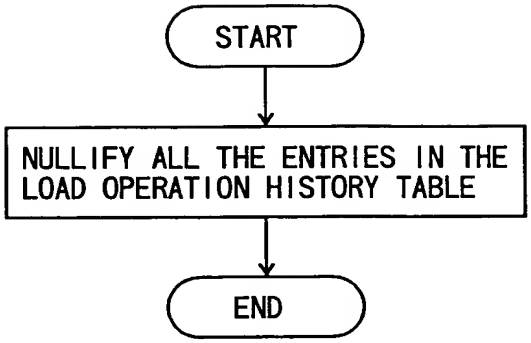


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FIG. 20

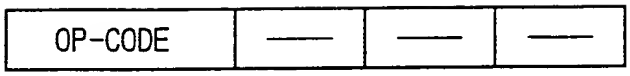

FIG.21

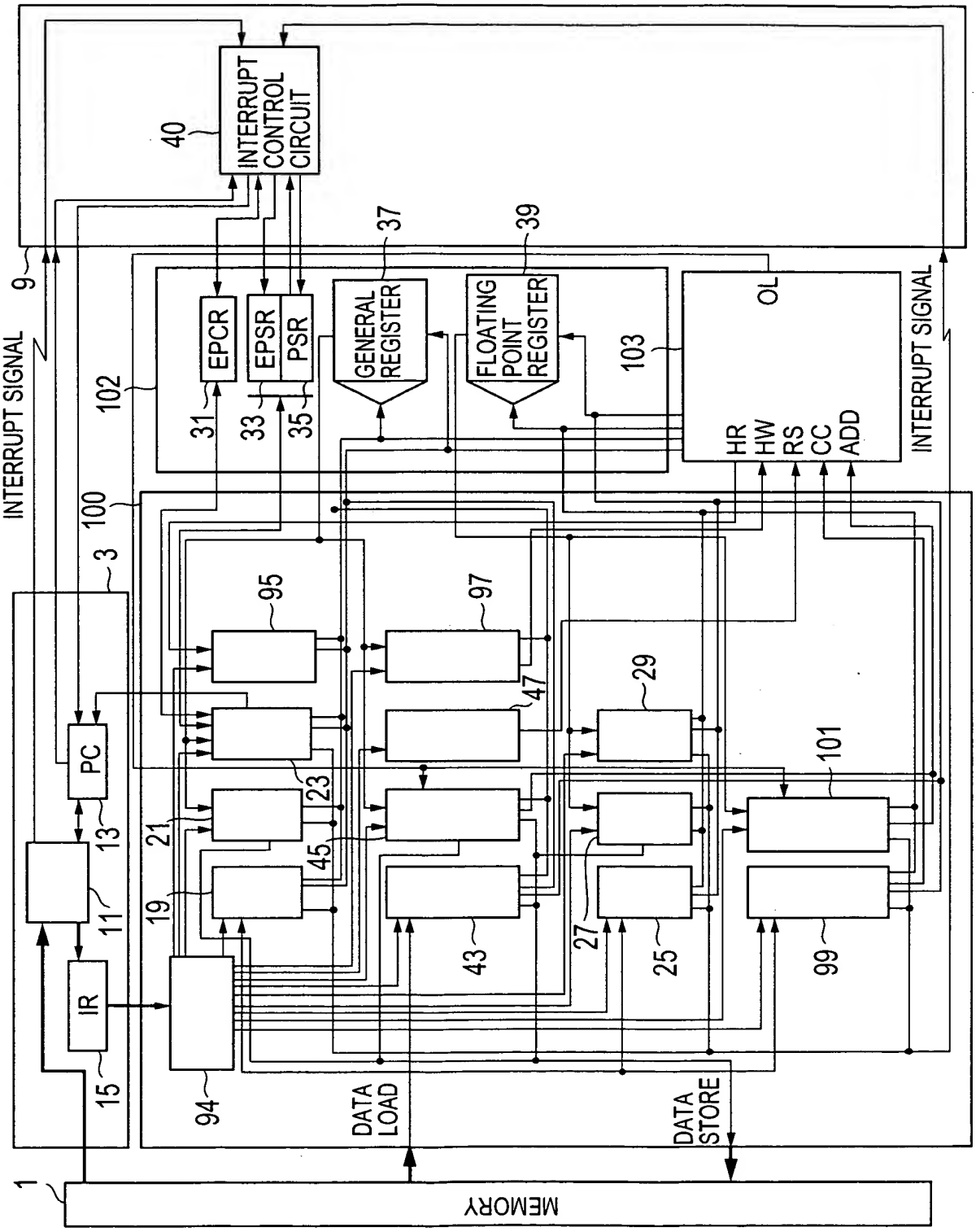
INTERRUPT CONTROL CIRCUIT
40
INTERRUPT SIGNAL
9
EPCR
EPSR
PSR
31
33
35
GENERAL REGISTER
37
FLOATING POINT REGISTER
39
102
103
OL
HR
HW
RS
CC
ADD
INTERRUPT SIGNAL
100
3
95
97
47
29
101
23
21
45
19
11
13
PC
IR
15
94
43
27
25
99
DATA LOAD
DATA STORE
1
MEMORY

FIG.22

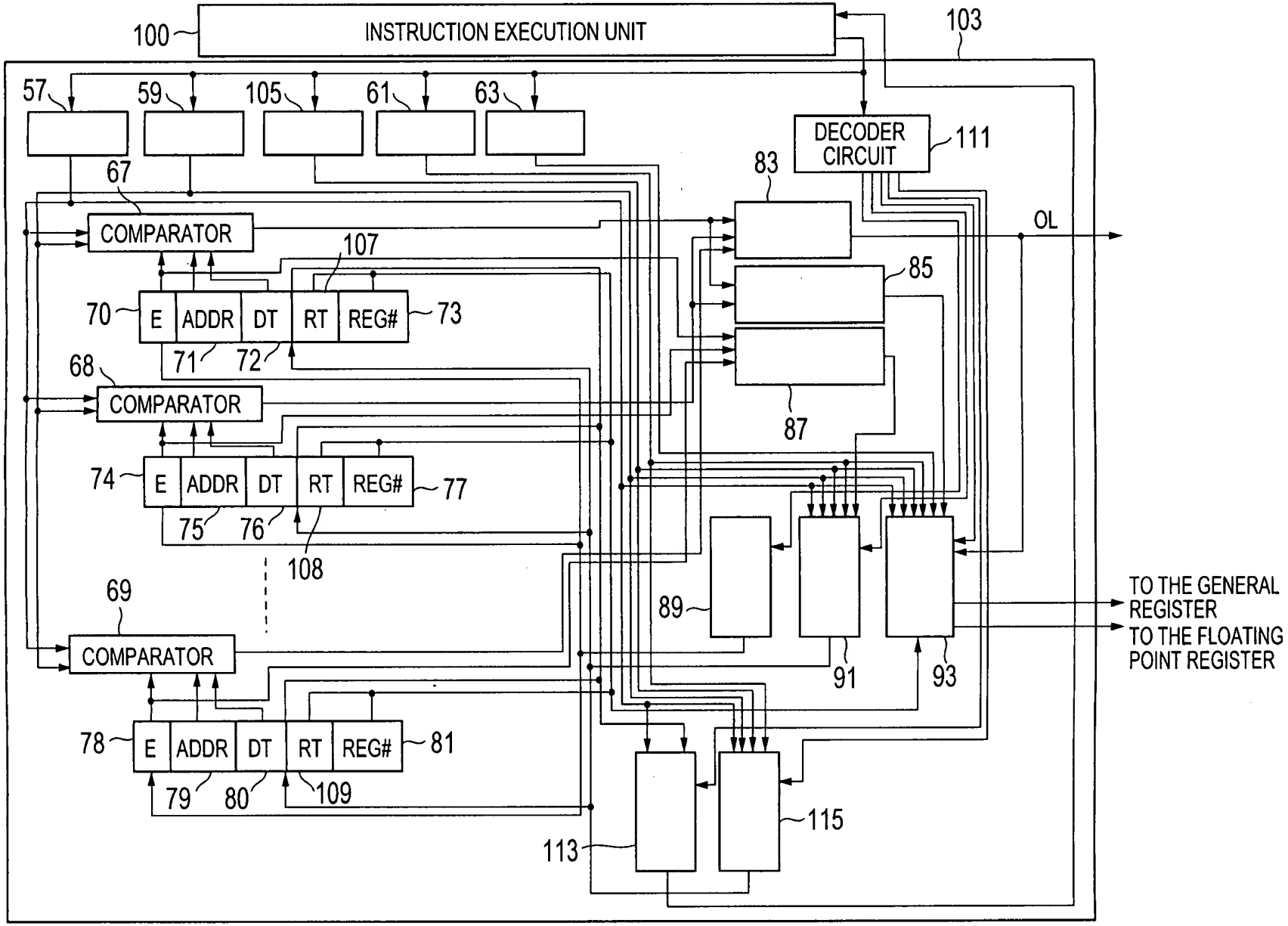
100
INSTRUCTION EXECUTION UNIT
103
57
59
105
61
63
DECODER CIRCUIT
111
67
83
COMPARATOR
OL
107
85
70
E
ADDR
DT
RT
REG#
73
71
72
68
COMPARATOR
87
74
E
ADDR
DT
RT
REG#
77
75
76
108
69
89
TO THE GENERAL REGISTER
TO THE FLOATING POINT REGISTER
COMPARATOR
91
93
78
E
ADDR
DT
RT
REG#
81
79
80
109
115
113

FIG.23

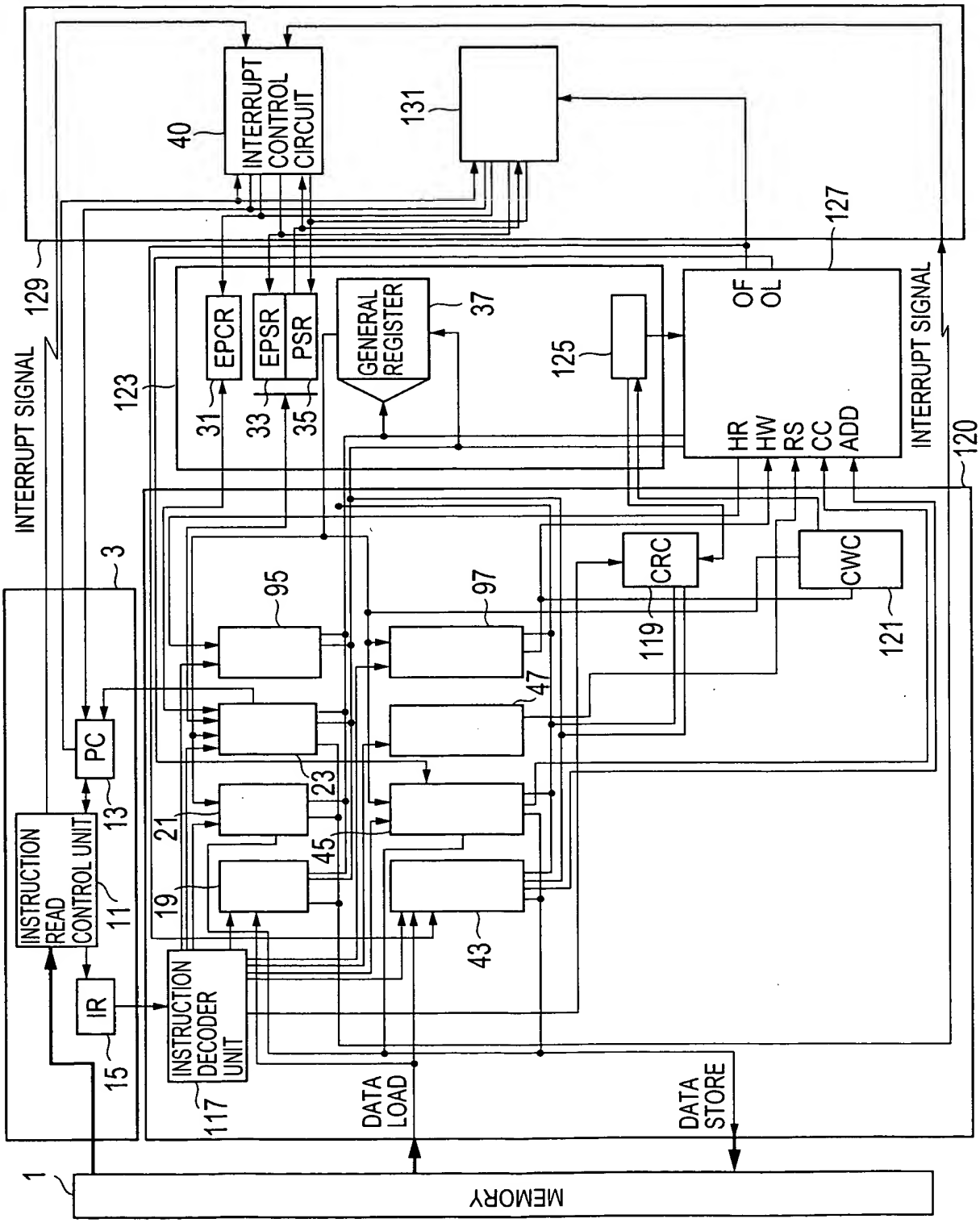
MEMORY
1
DATA LOAD
DATA STORE
INSTRUCTION DECODER UNIT
117
IR
15
INSTRUCTION READ CONTROL UNIT
11
PC
13
3
INTERRUPT SIGNAL
129
40
INTERRUPT CONTROL CIRCUIT
131
127
OF
OL
HR
HW
RS
CC
ADD
INTERRUPT SIGNAL
120
123
EPCR
EPSR
PSR
31
33
35
GENERAL REGISTER
37
125
CRC
119
CWC
121
95
97
47
23
21
45
19
43

FIG.24

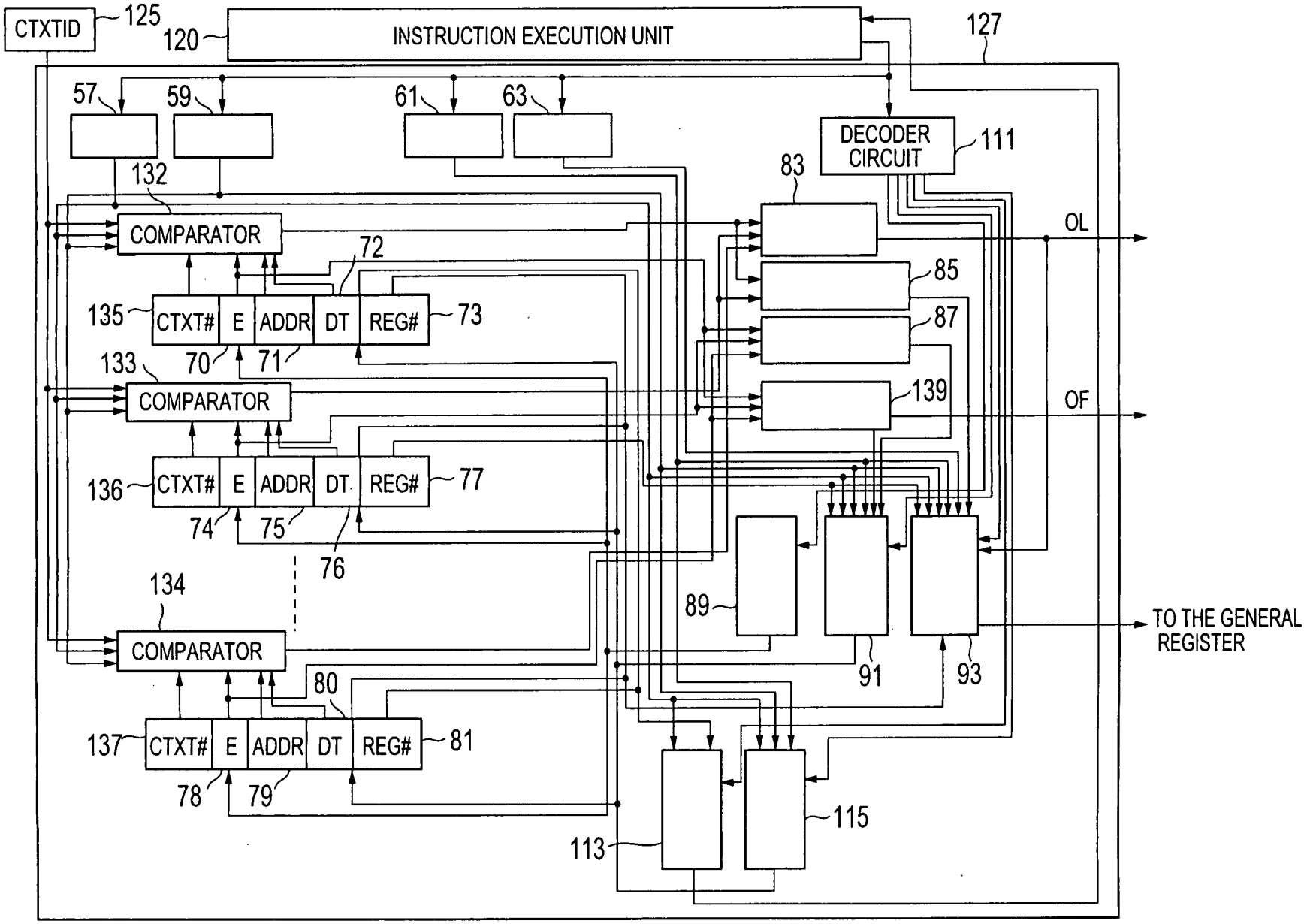
CTXTID
125
120
INSTRUCTION EXECUTION UNIT
127
57
59
61
63
DECODER CIRCUIT
111
83
132
COMPARATOR
72
OL
85
135
CTXT#
E
ADDR
DT
REG#
73
87
70
71
133
COMPARATOR
139
OF
136
CTXT#
E
ADDR
DT
REG#
77
74
75
76
134
89
TO THE GENERAL REGISTER
COMPARATOR
91
93
80
137
CTXT#
E
ADDR
DT
REG#
81
78
79
115
113

FIG.25

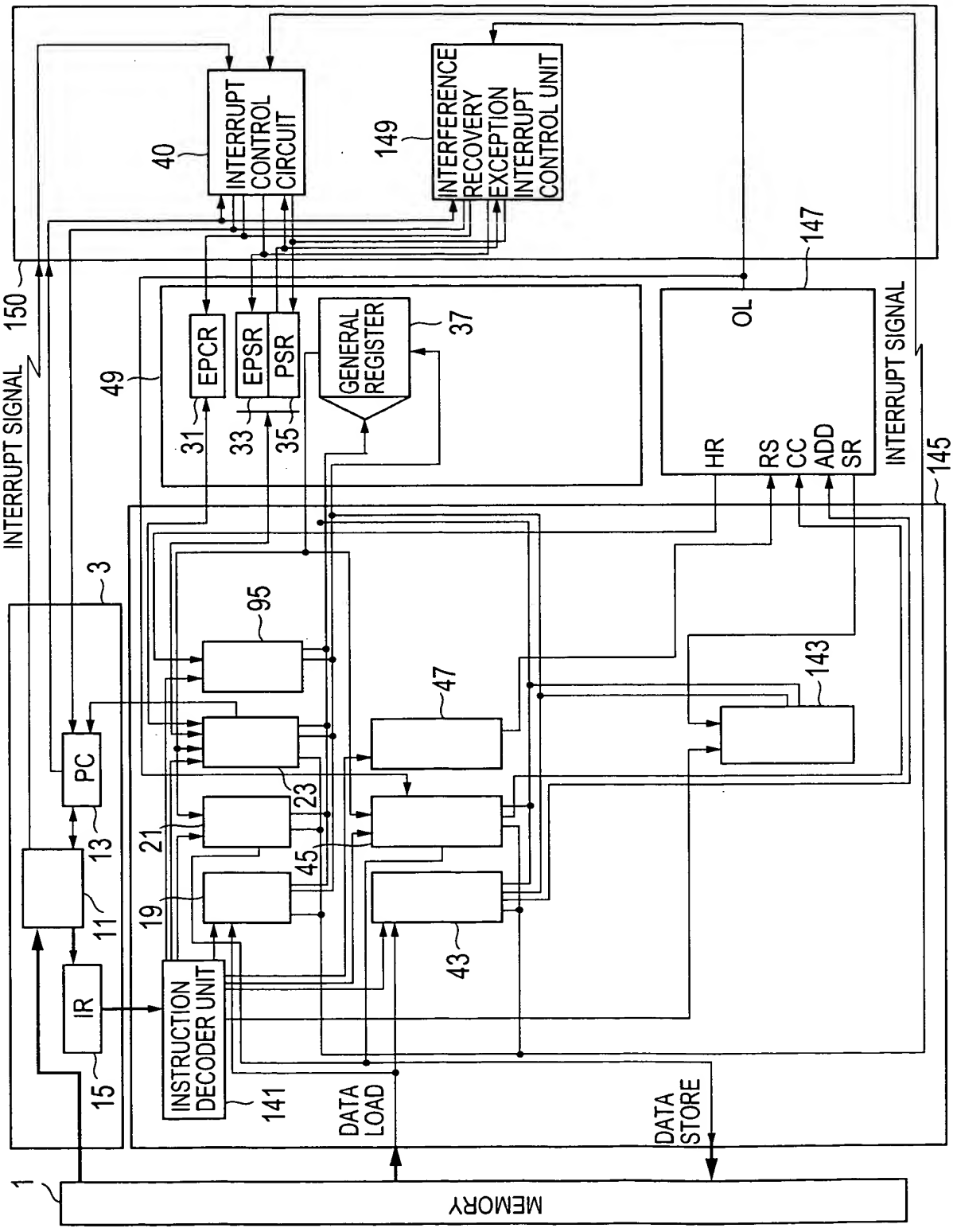
INTERRUPT CONTROL CIRCUIT
40
INTERFERENCE RECOVERY EXCEPTION INTERRUPT CONTROL UNIT
149
147
150
INTERRUPT SIGNAL
49
EPCR
EPSR
PSR
GENERAL REGISTER
37
31
33
35
OL
HR
RS
CC
ADD
SR
INTERRUPT SIGNAL
145
3
95
47
143
PC
13
21
23
45
19
11
IR
15
INSTRUCTION DECODER UNIT
141
43
DATA LOAD
DATA STORE
1
MEMORY

FIG.26

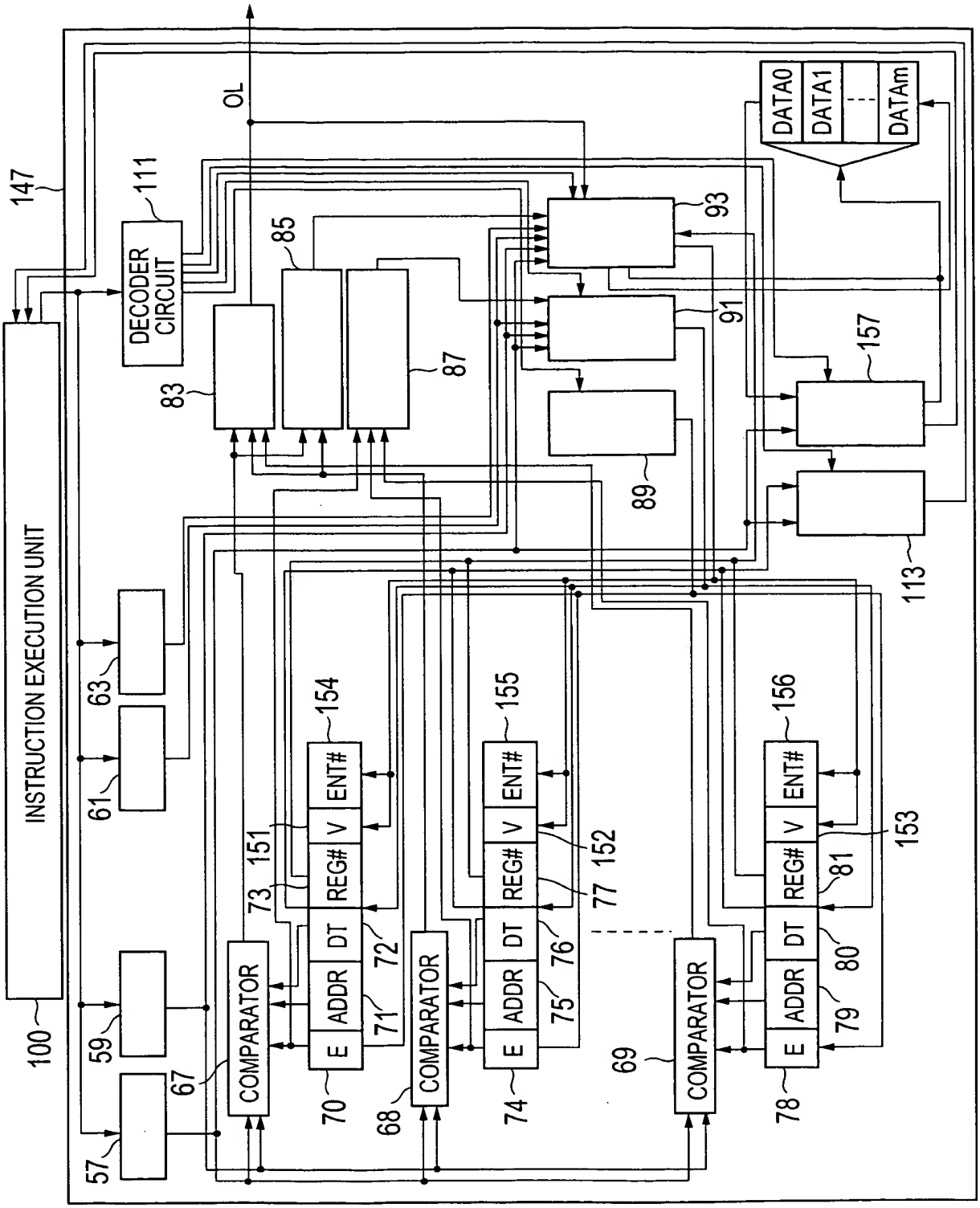
INSTRUCTION EXECUTION UNIT
100
147
DECODER CIRCUIT
111
OL
DATA0
DATA1
DATAm
83
85
87
89
91
93
113
157
57
59
61
63
67
69
COMPARATOR
70
71
72
73
74
75
76
77
78
79
80
81
151
152
153
154
155
156
E
ADDR
DT
REG#
V
ENT#

FIG. 27

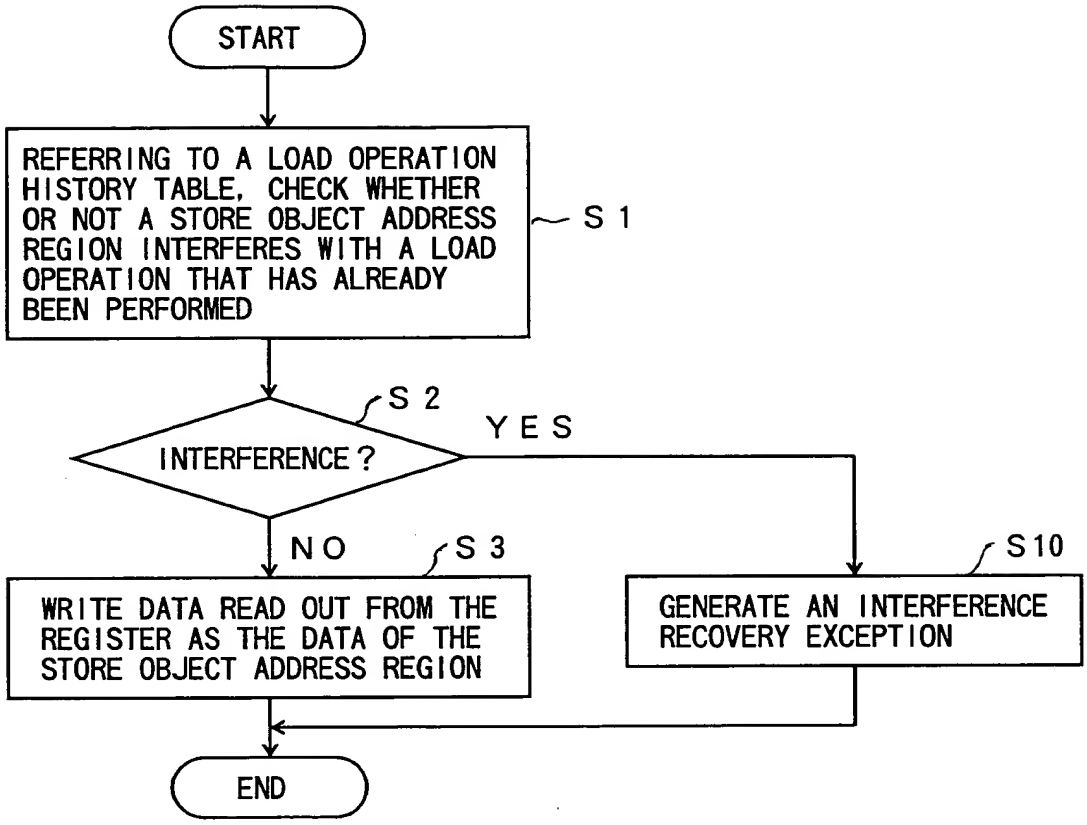
START
REFERRING TO A LOAD OPERATION HISTORY TABLE, CHECK WHETHER OR NOT A STORE OBJECT ADDRESS REGION INTERFERES WITH A LOAD OPERATION THAT HAS ALREADY BEEN PERFORMED
S 1
S 2
INTERFERENCE ?
YES
NO
S 3
WRITE DATA READ OUT FROM THE REGISTER AS THE DATA OF THE STORE OBJECT ADDRESS REGION
S10
GENERATE AN INTERFERENCE RECOVERY EXCEPTION
END

FIG. 28

FIG. 29

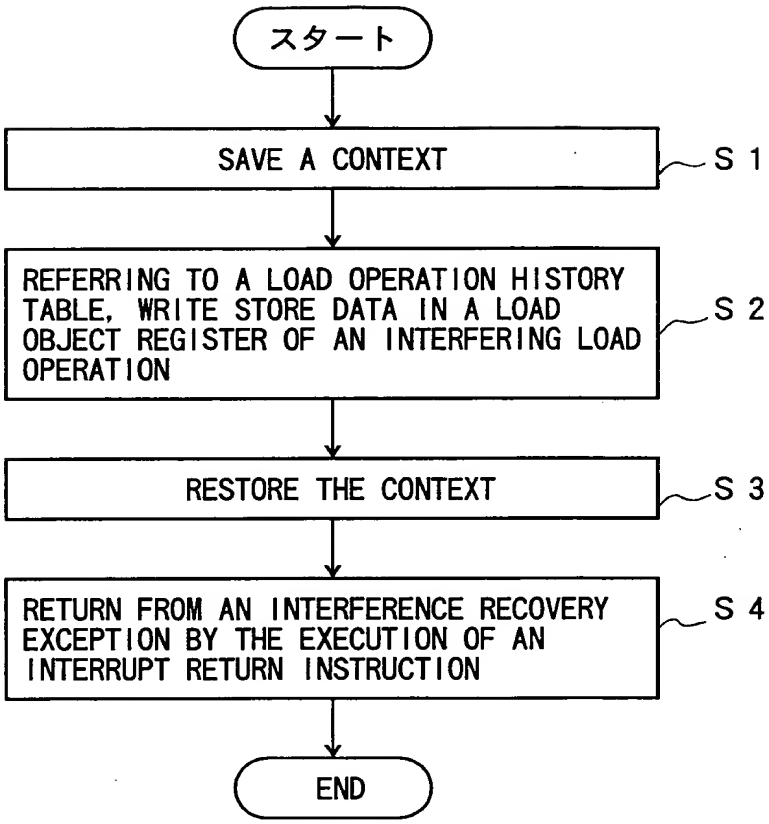
スタート
SAVE A CONTEXT
S 1
REFERRING TO A LOAD OPERATION HISTORY TABLE, WRITE STORE DATA IN A LOAD OBJECT REGISTER OF AN INTERFERING LOAD OPERATION
S 2
RESTORE THE CONTEXT
S 3
RETURN FROM AN INTERFERENCE RECOVERY EXCEPTION BY THE EXECUTION OF AN INTERRUPT RETURN INSTRUCTION
S 4
END

FIG.30

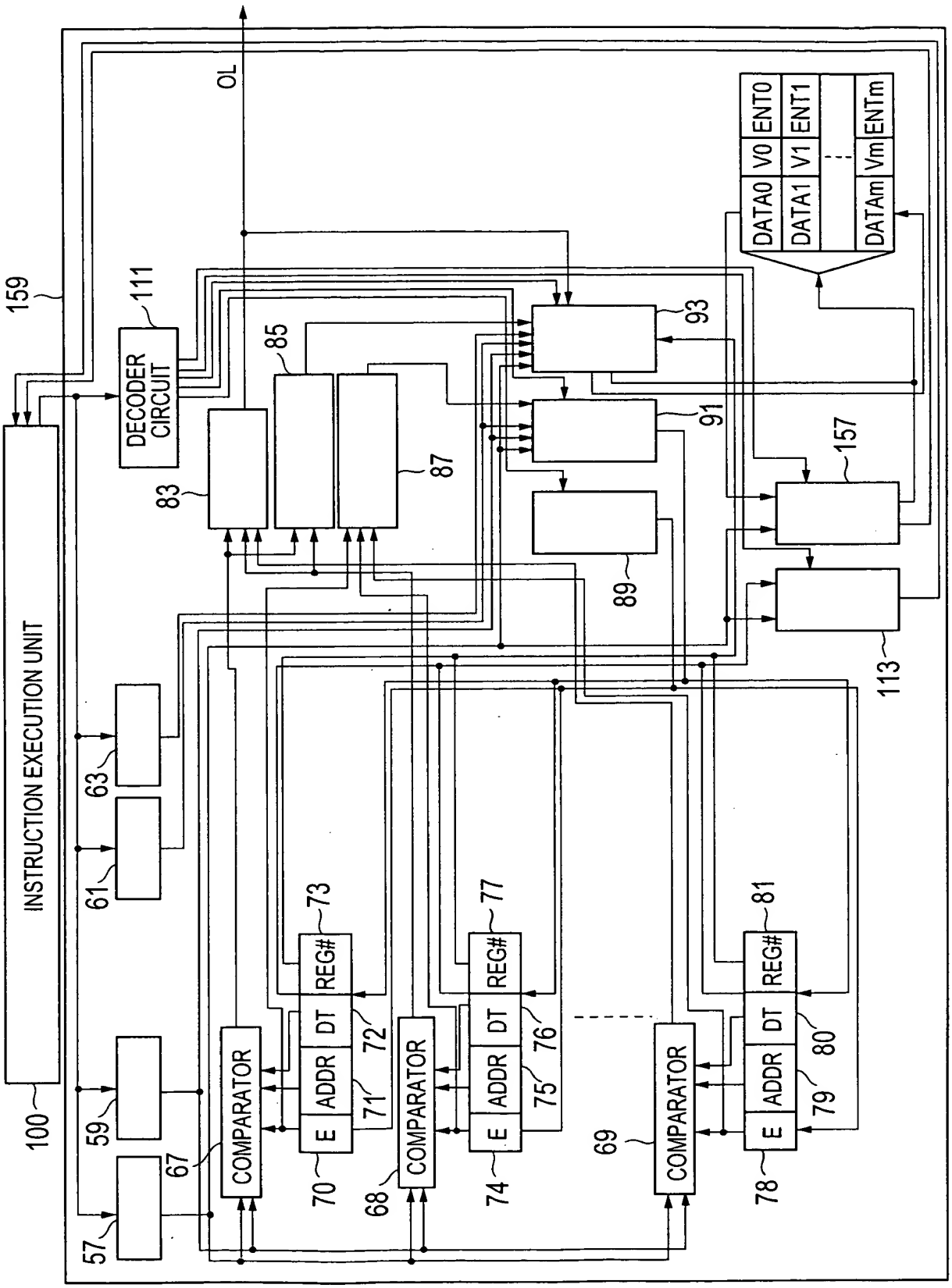
INSTRUCTION EXECUTION UNIT
100
159
DECODER CIRCUIT
111
OL
DATA0
DATA1
DATAm
V0
V1
Vm
ENT0
ENT1
ENTm
83
85
87
89
91
93
157
113
57
59
61
63
67
69
COMPARATOR
E
ADDR
DT
REG#
70
71
72
73
74
75
76
77
78
79
80
81

FIG.31

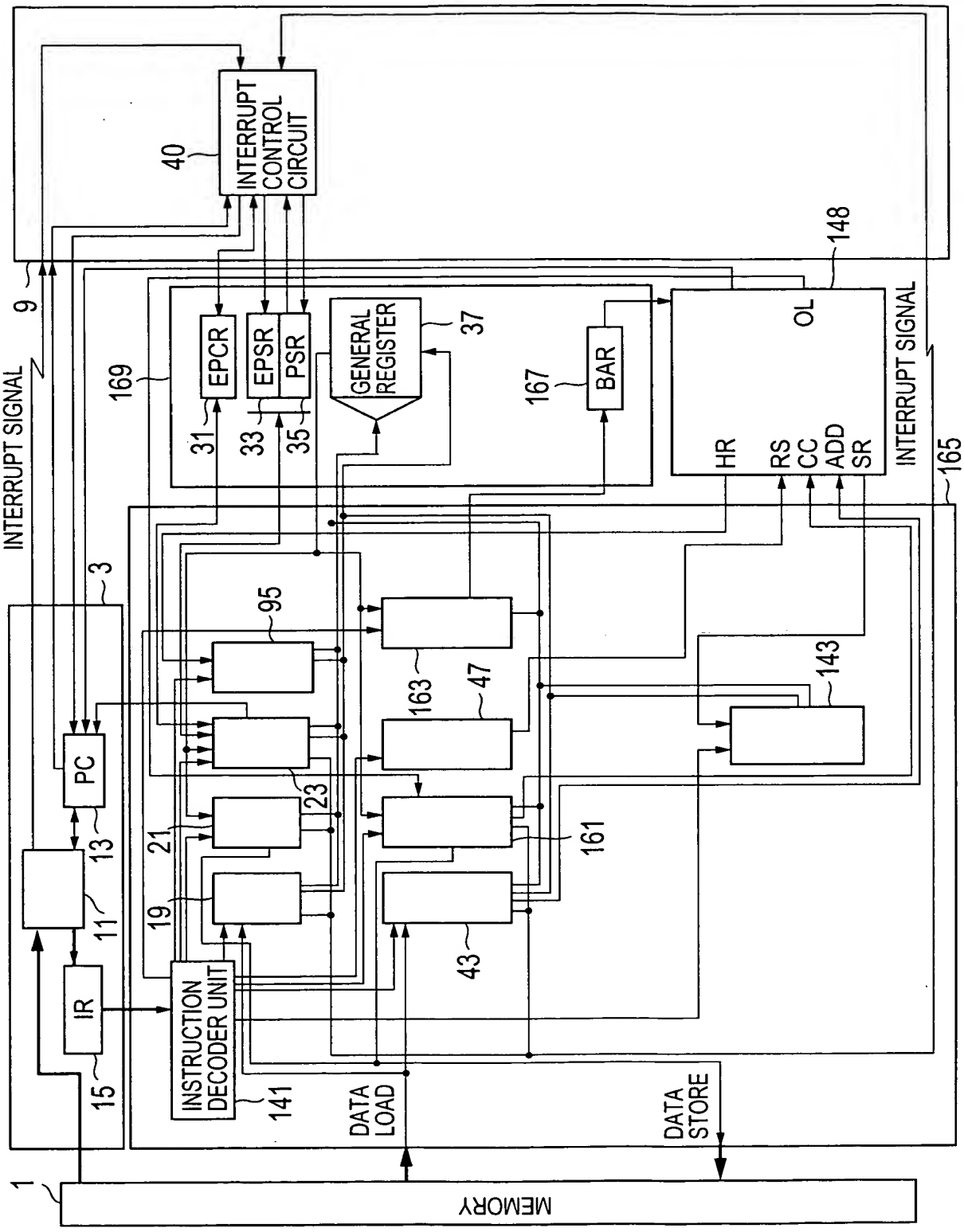
INTERRUPT CONTROL CIRCUIT
40
INTERRUPT SIGNAL
9
169
EPCR
EPSR
PSR
31
33
35
GENERAL REGISTER
37
167
BAR
148
OL
HR
RS
CC
ADD
SR
INTERRUPT SIGNAL
165
3
95
PC
13
11
IR
15
INSTRUCTION DECODER UNIT
141
21
19
23
163
47
143
161
43
DATA LOAD
DATA STORE
1
MEMORY

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FIG.32

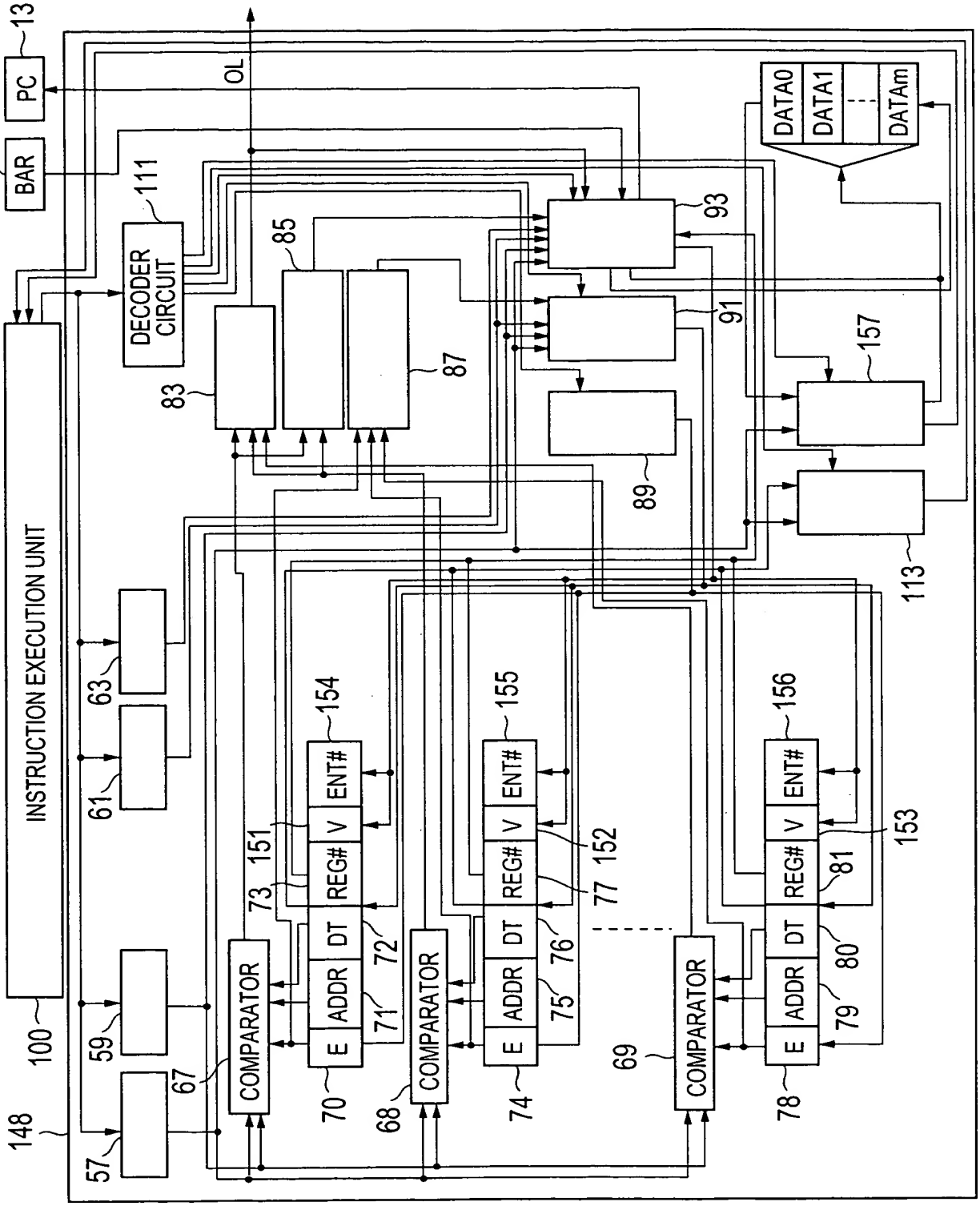

FIG. 33

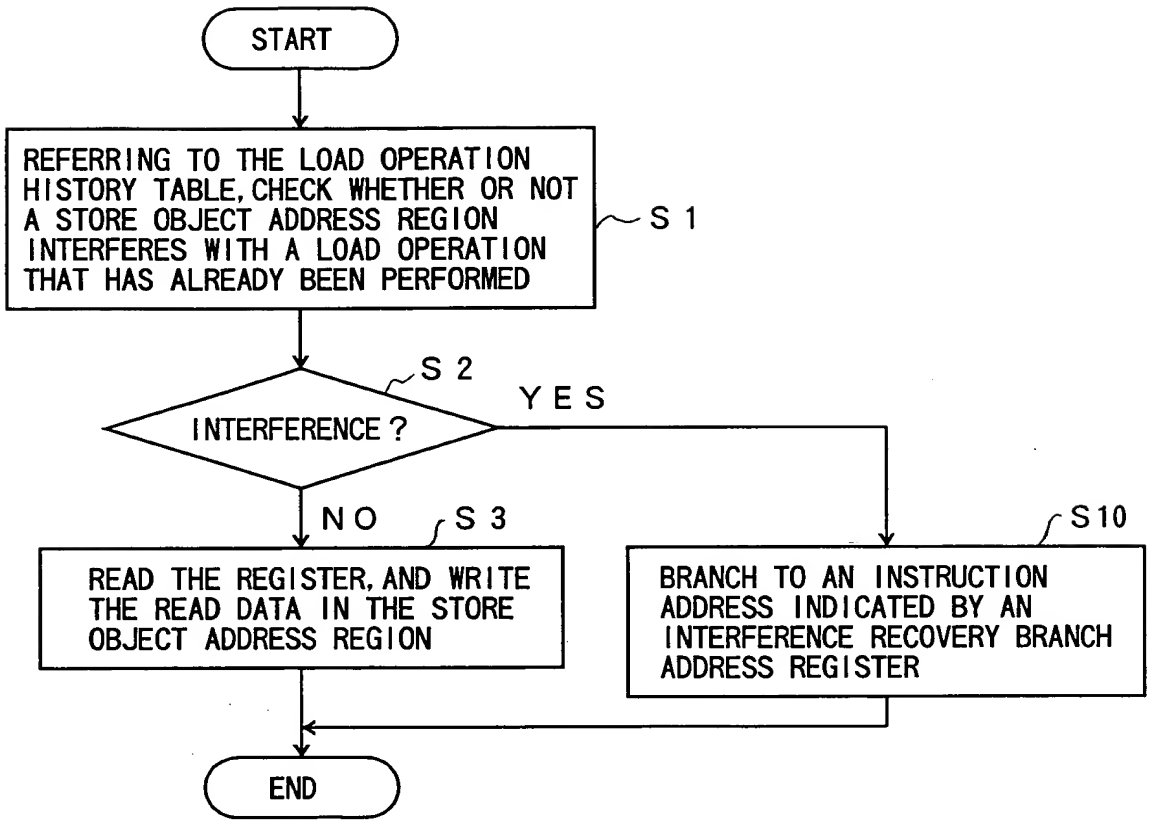
START
REFERRING TO THE LOAD OPERATION HISTORY TABLE, CHECK WHETHER OR NOT A STORE OBJECT ADDRESS REGION INTERFERES WITH A LOAD OPERATION THAT HAS ALREADY BEEN PERFORMED
S 1
S 2
INTERFERENCE ?
YES
NO
S 3
READ THE REGISTER, AND WRITE THE READ DATA IN THE STORE OBJECT ADDRESS REGION
S10
BRANCH TO AN INSTRUCTION ADDRESS INDICATED BY AN INTERFERENCE RECOVERY BRANCH ADDRESS REGISTER
END

FIG. 34

0 5 5 0 4 1 2 5 4 5 3 5 0 2 0

FIG.35

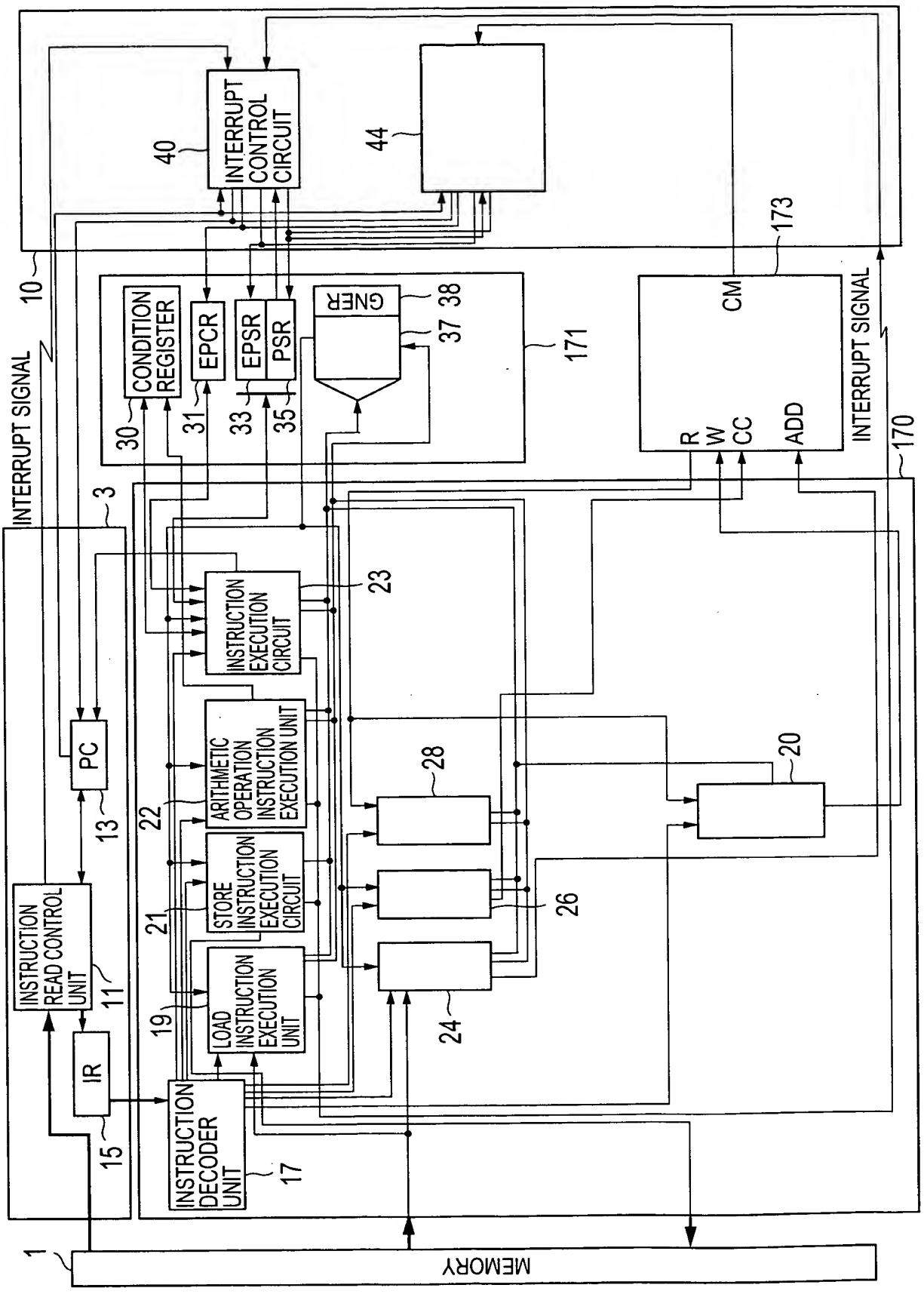
MEMORY
1
INSTRUCTION SIGNAL
10
INTERRUPT CONTROL CIRCUIT
40
44
CONDITION REGISTER
30
EPCR
31
EPSR
33
PSR
35
GNFR
37 38
171
CM
173
R
W
CC
ADD
INTERRUPT SIGNAL
170
3
INSTRUCTION EXECUTION CIRCUIT
23
PC
13
ARITHMETIC OPERATION INSTRUCTION EXECUTION UNIT
22
28
20
STORE INSTRUCTION EXECUTION CIRCUIT
21
26
INSTRUCTION READ CONTROL UNIT
11
LOAD INSTRUCTION EXECUTION UNIT
19
24
IR
15
INSTRUCTION DECODER UNIT
17

FIG.36

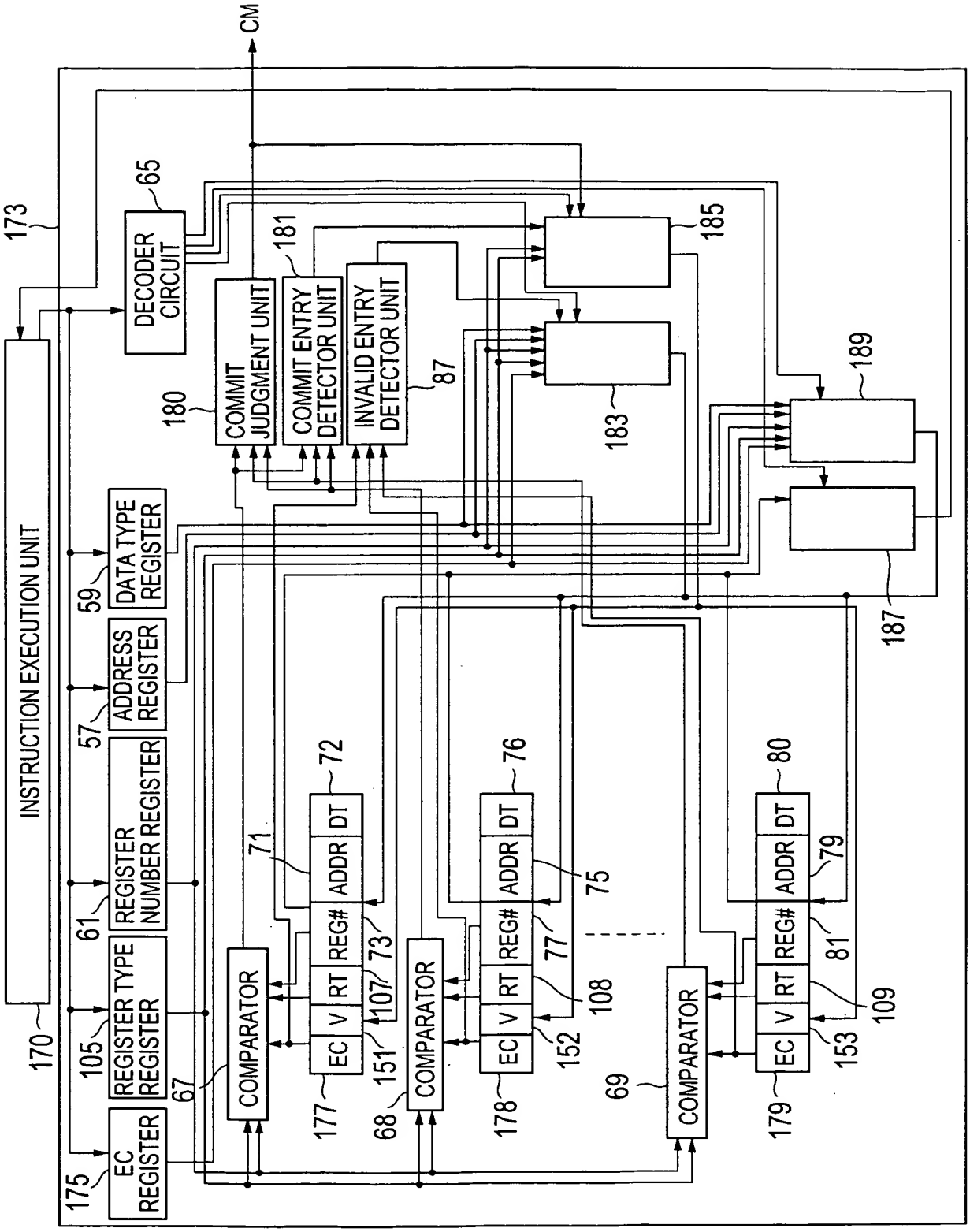
CM
173
DECODER CIRCUIT
65
COMMIT JUDGMENT UNIT
180
COMMIT ENTRY DETECTOR UNIT
181
INVALID ENTRY DETECTOR UNIT
87
185
183
189
187
INSTRUCTION EXECUTION UNIT
170
DATA TYPE REGISTER
59
ADDRESS REGISTER
57
REGISTER NUMBER REGISTER
61
REGISTER TYPE REGISTER
105
EC REGISTER
175
67
COMPARATOR
71
72
DT
ADDR
REG#
RT
V
EC
177
73
107
151
68
COMPARATOR
76
75
77
108
152
178
69
COMPARATOR
80
79
81
109
153
179

FIG. 37

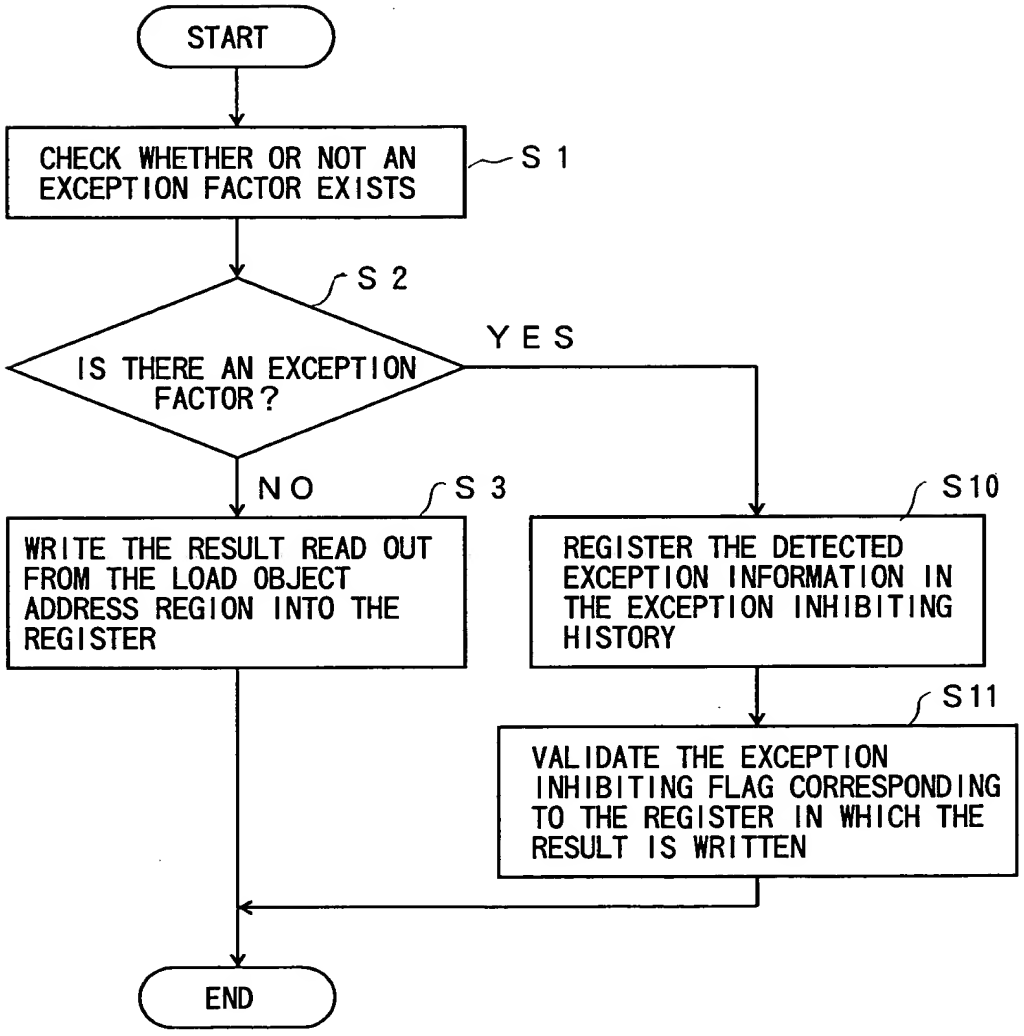

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FIG. 38

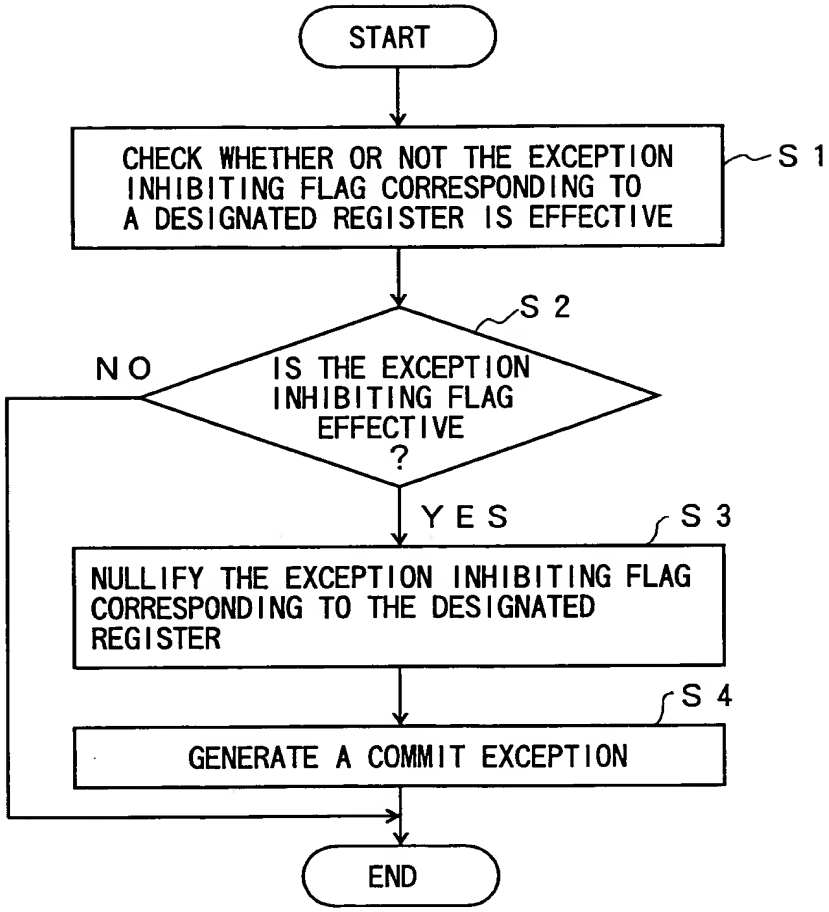

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FIG. 39

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FIG.40

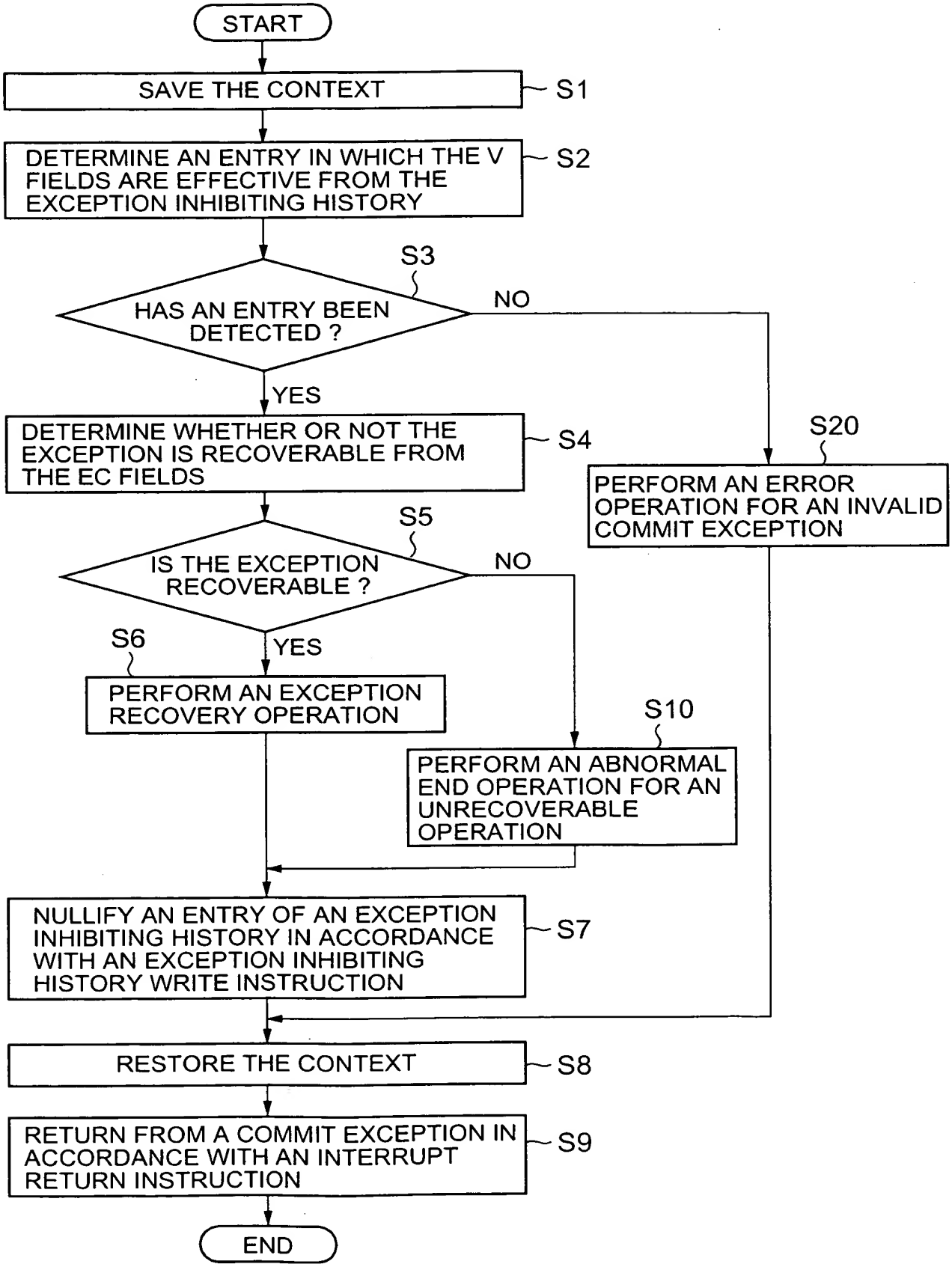
START
SAVE THE CONTEXT
S1
DETERMINE AN ENTRY IN WHICH THE V FIELDS ARE EFFECTIVE FROM THE EXCEPTION INHIBITING HISTORY
S2
S3
HAS AN ENTRY BEEN DETECTED ?
NO
YES
DETERMINE WHETHER OR NOT THE EXCEPTION IS RECOVERABLE FROM THE EC FIELDS
S4
S20
PERFORM AN ERROR OPERATION FOR AN INVALID COMMIT EXCEPTION
S5
IS THE EXCEPTION RECOVERABLE ?
NO
S6
YES
PERFORM AN EXCEPTION RECOVERY OPERATION
S10
PERFORM AN ABNORMAL END OPERATION FOR AN UNRECOVERABLE OPERATION
NULLIFY AN ENTRY OF AN EXCEPTION INHIBITING HISTORY IN ACCORDANCE WITH AN EXCEPTION INHIBITING HISTORY WRITE INSTRUCTION
S7
RESTORE THE CONTEXT
S8
RETURN FROM A COMMIT EXCEPTION IN ACCORDANCE WITH AN INTERRUPT RETURN INSTRUCTION
S9
END

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FIG.41

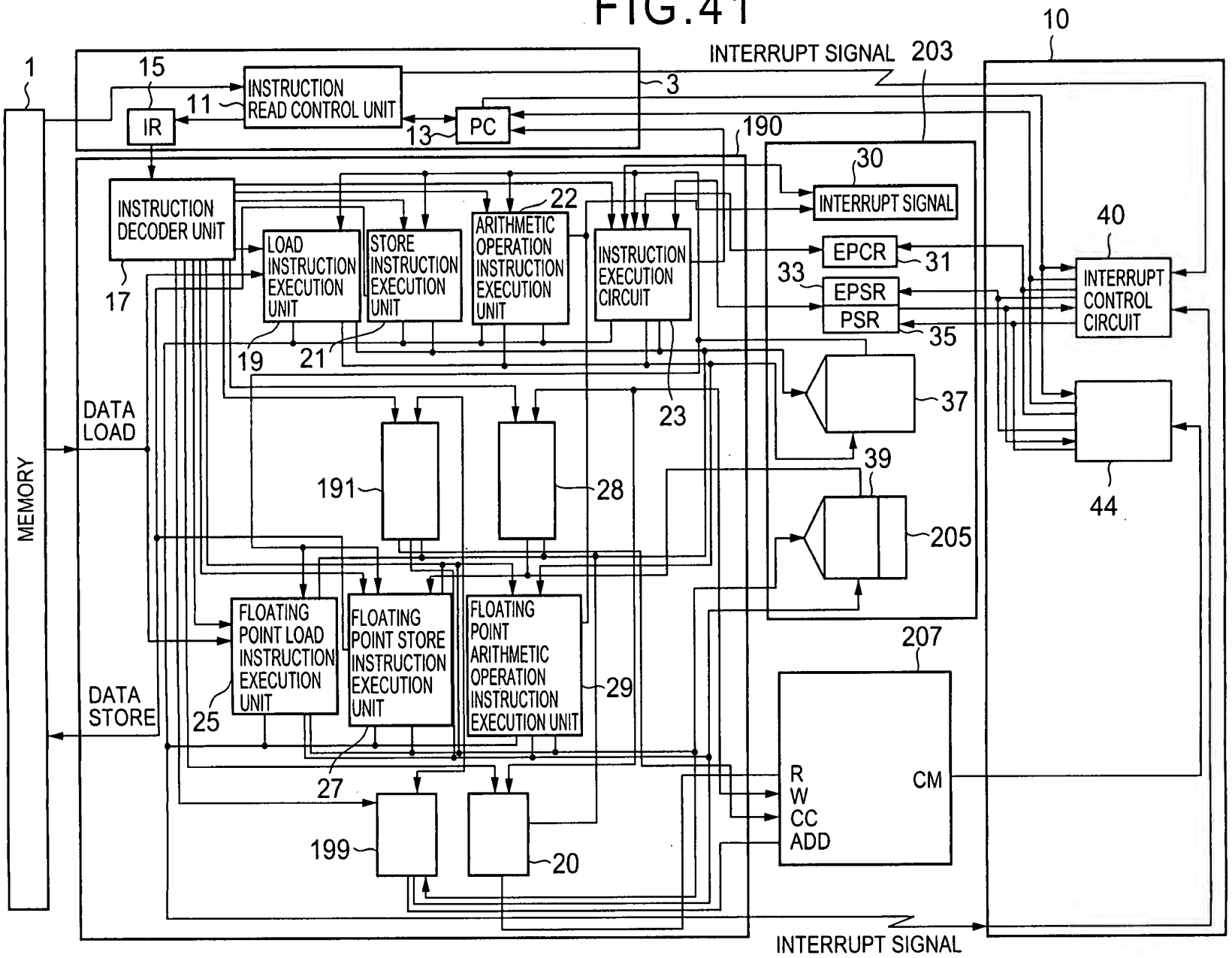

FIG.42

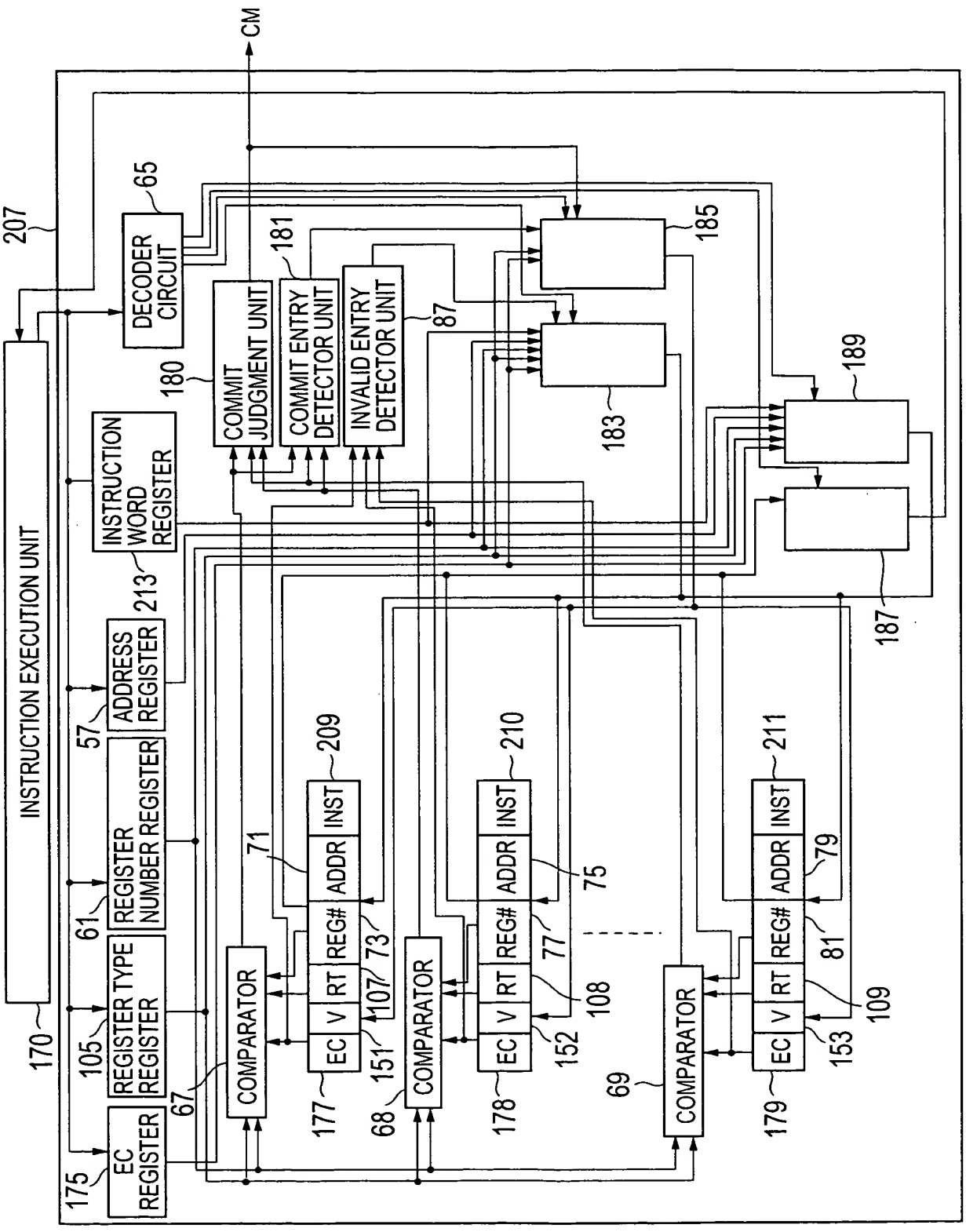
CM
207
65
DECODER CIRCUIT
181
185
COMMIT JUDGMENT UNIT
COMMIT ENTRY DETECTOR UNIT
INVALID ENTRY DETECTOR UNIT
87
180
183
189
INSTRUCTION WORD REGISTER
213
187
INSTRUCTION EXECUTION UNIT
ADDRESS REGISTER
57
REGISTER NUMBER REGISTER
61
REGISTER TYPE REGISTER
105
EC REGISTER
175
170
71
209
210
211
INST
ADDR
REG#
RT
V
EC
75
77
73
107
79
81
109
108
152
153
151
177
178
179
67
68
69
COMPARATOR
COMPARATOR
COMPARATOR

FIG. 43

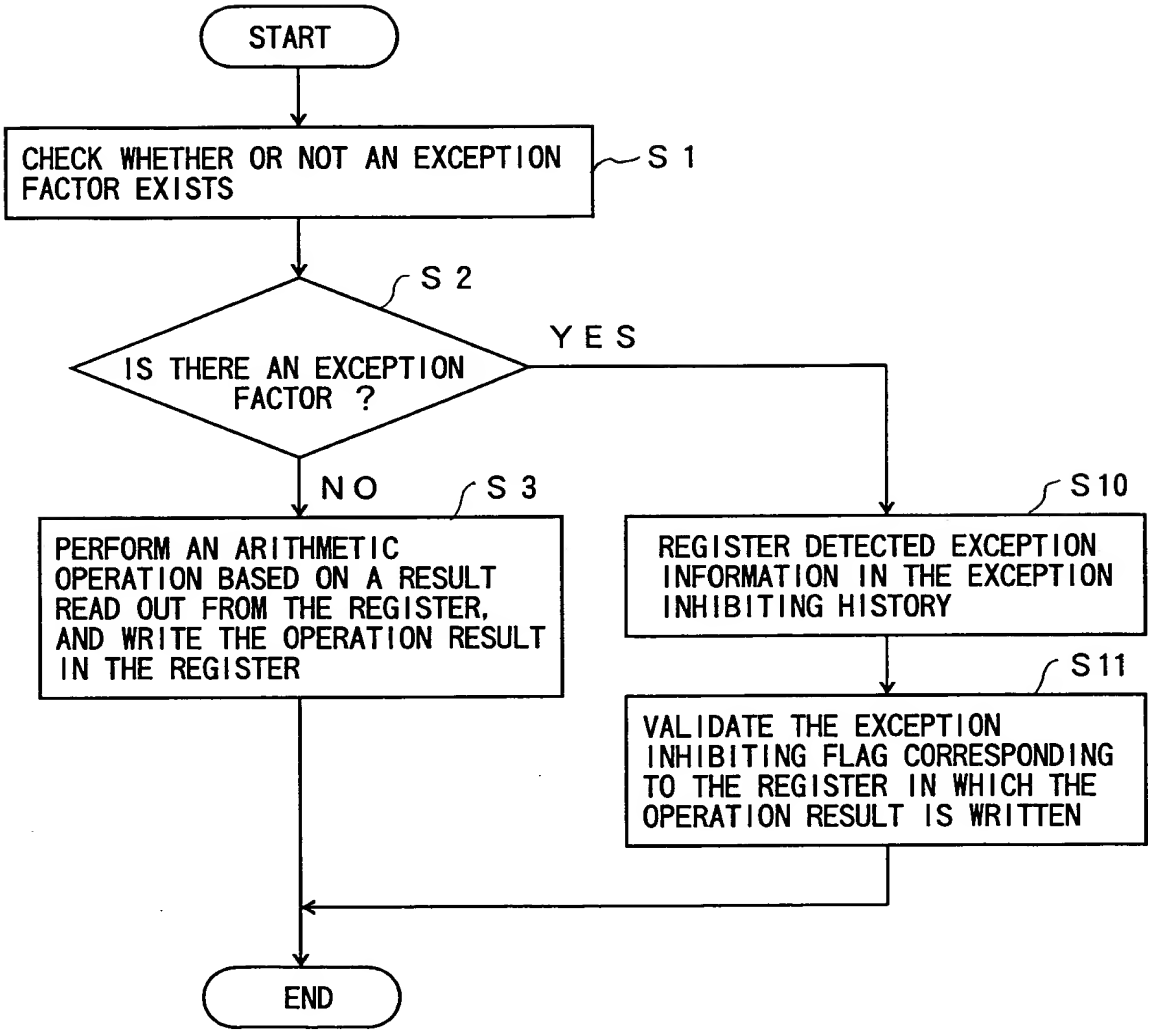

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FIG.44

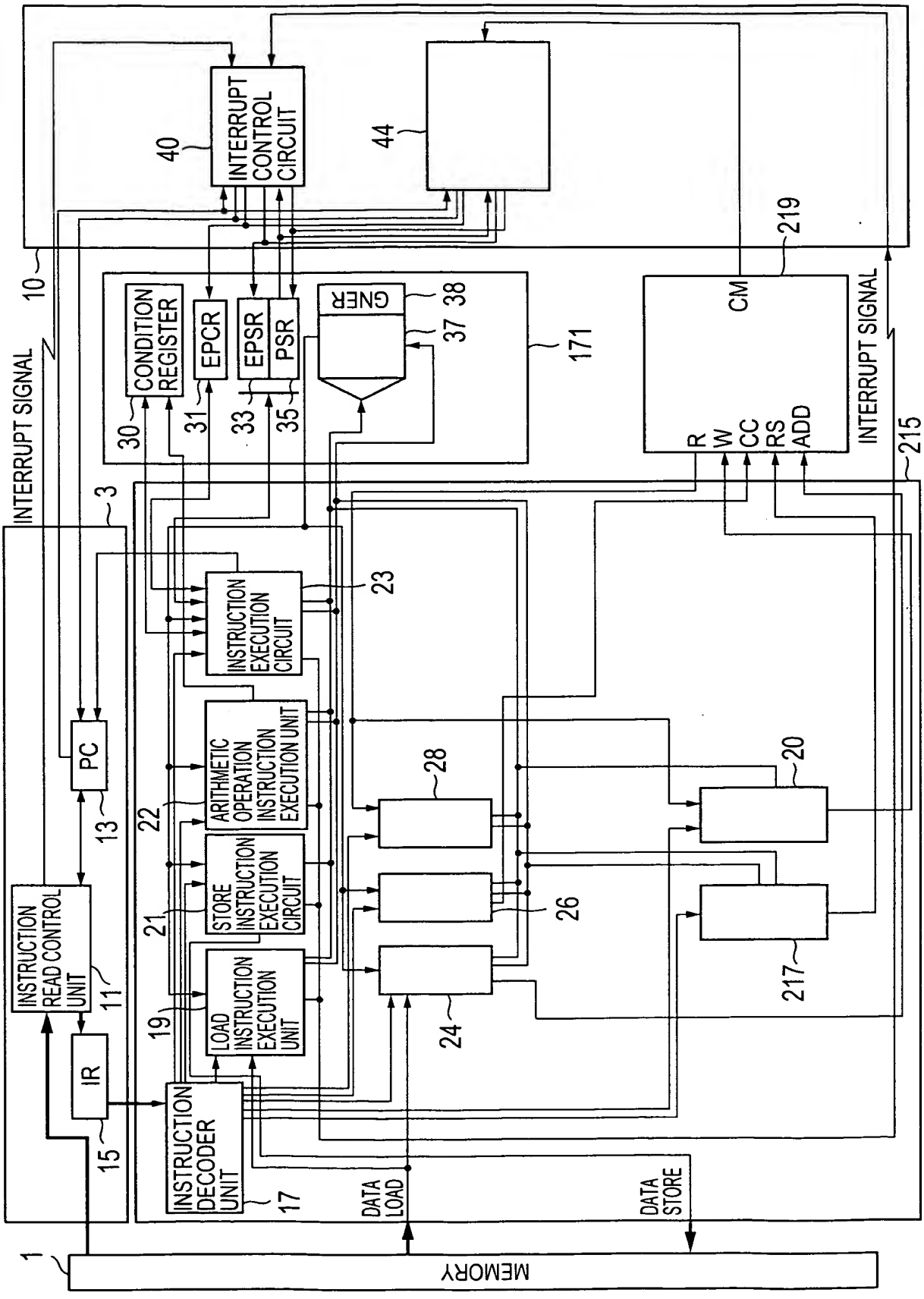
MEMORY
1
DATA LOAD
DATA STORE
INSTRUCTION DECODER UNIT
17
IR
15
INSTRUCTION READ CONTROL UNIT
11
PC
13
3
INTERRUPT SIGNAL
10
LOAD INSTRUCTION EXECUTION UNIT
19
STORE INSTRUCTION EXECUTION CIRCUIT
21
ARITHMETIC OPERATION INSTRUCTION EXECUTION UNIT
22
INSTRUCTION EXECUTION CIRCUIT
23
24
26
28
20
217
CONDITION REGISTER
30
EPCR
31
EPSR
33
PSR
35
GNER
37 38
171
INTERRUPT CONTROL CIRCUIT
40
44
CM
219
R
W
CC
RS
ADD
INTERRUPT SIGNAL
215

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FIG.45

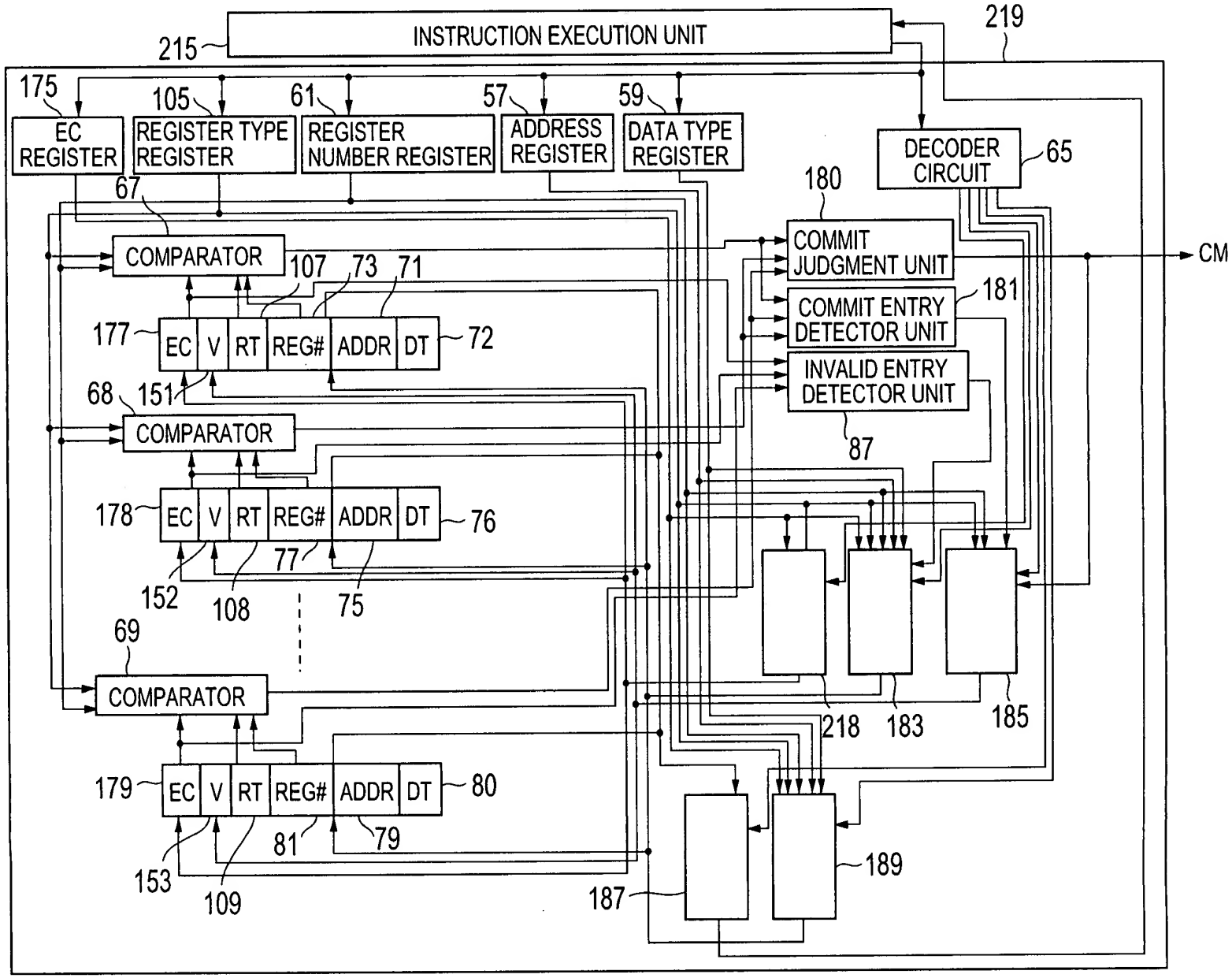

FIG. 46

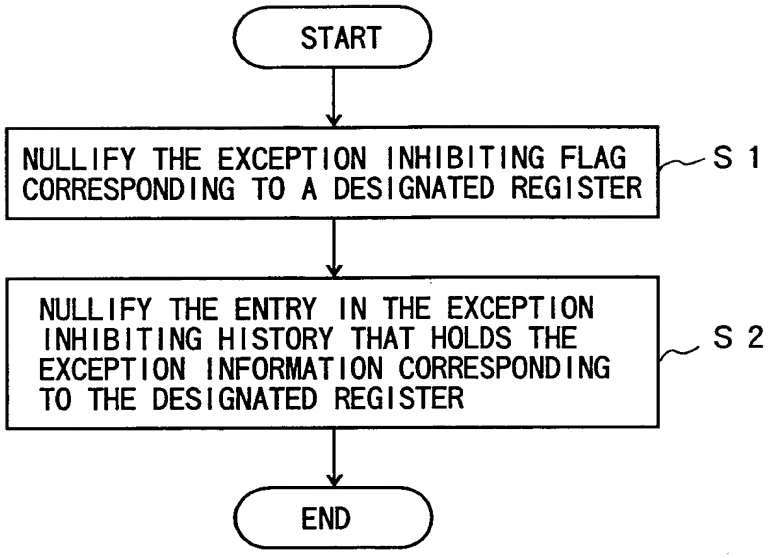

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FIG.47

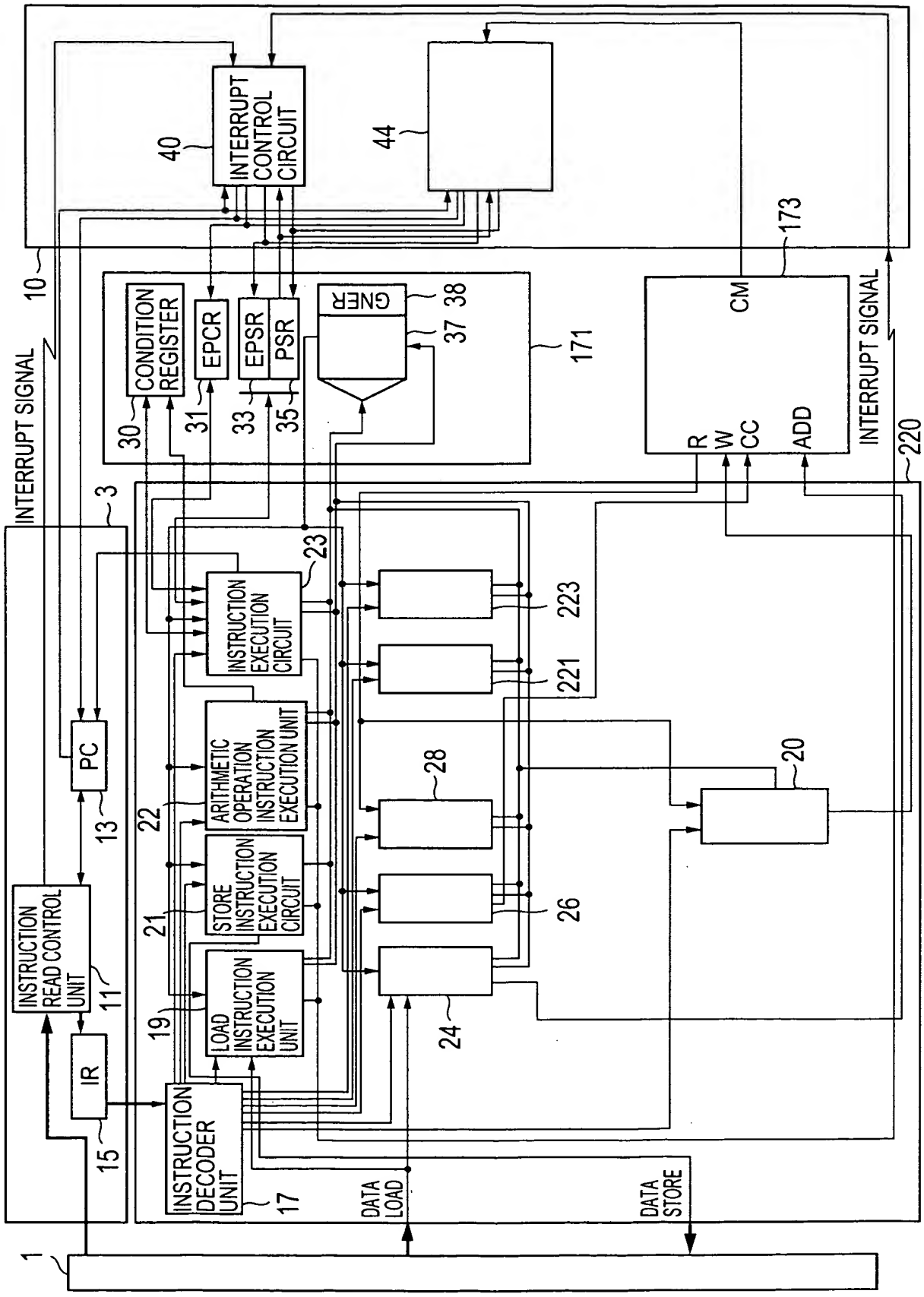
INTERRUPT CONTROL CIRCUIT
40
44
10
INTERRUPT SIGNAL
CONDITION REGISTER
30
EPCR
31
EPSR
33
PSR
35
GNER
37 38
171
CM
173
R
W
CC
ADD
INTERRUPT SIGNAL
220
3
INSTRUCTION EXECUTION CIRCUIT
23
223
221
PC
13
ARITHMETIC OPERATION INSTRUCTION EXECUTION UNIT
22
28
20
STORE INSTRUCTION EXECUTION CIRCUIT
21
26
INSTRUCTION READ CONTROL UNIT
11
LOAD INSTRUCTION EXECUTION UNIT
19
24
IR
15
INSTRUCTION DECODER UNIT
17
DATA LOAD
DATA STORE
1

FIG.48

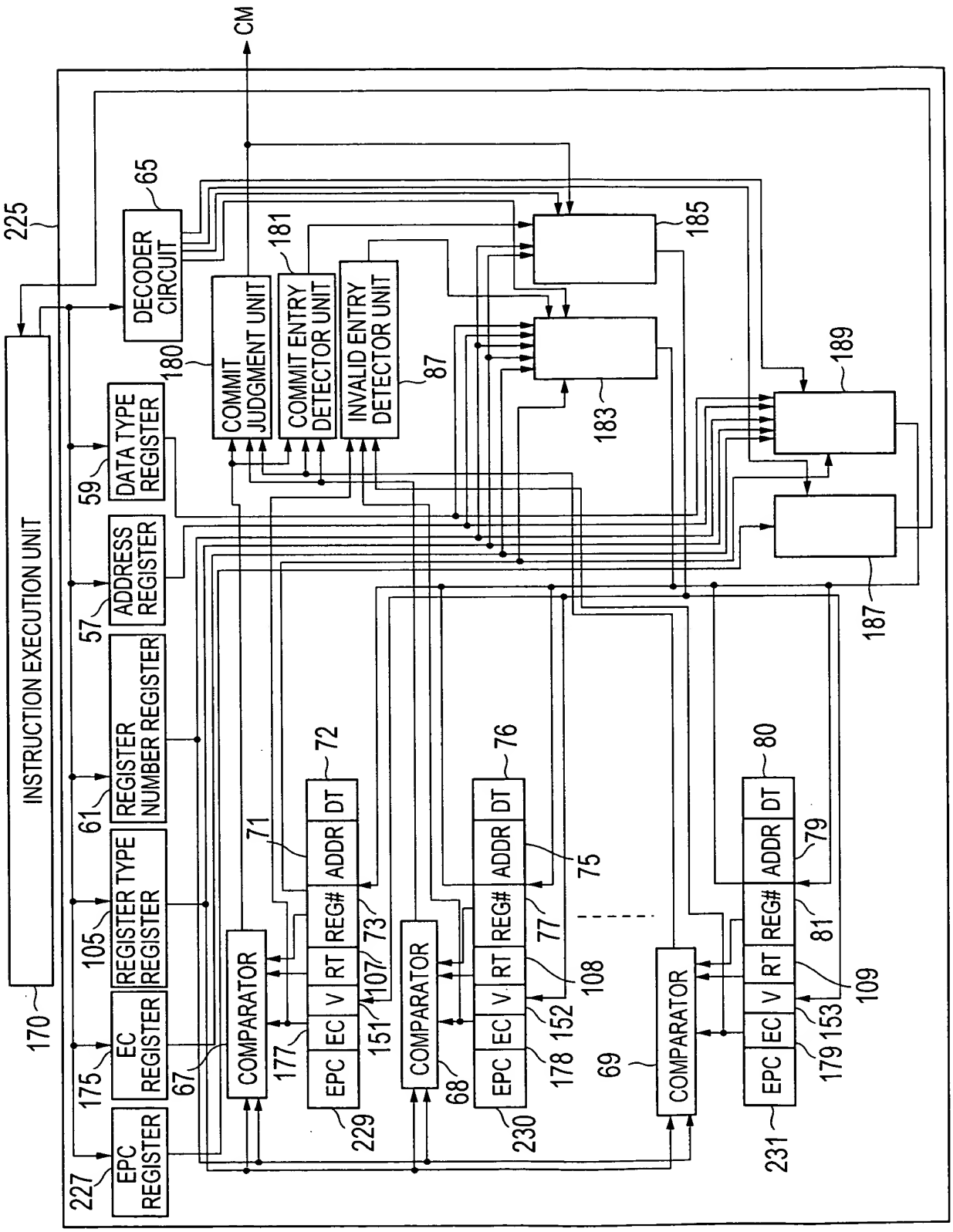
INSTRUCTION EXECUTION UNIT
170
225
CM
DECODER CIRCUIT
65
COMMIT JUDGMENT UNIT
180
COMMIT ENTRY DETECTOR UNIT
181
INVALID ENTRY DETECTOR UNIT
87
185
183
189
187
DATA TYPE REGISTER
59
ADDRESS REGISTER
57
REGISTER NUMBER REGISTER
61
REGISTER TYPE REGISTER
105
EC REGISTER
175
EPC REGISTER
227
COMPARATOR
67
71
177
EPC
EC
V
RT
REG#
ADDR
DT
72
229
151
107
73
COMPARATOR
68
76
230
178
152
108
77
75
COMPARATOR
69
80
231
179
153
109
81
79

FIG.49

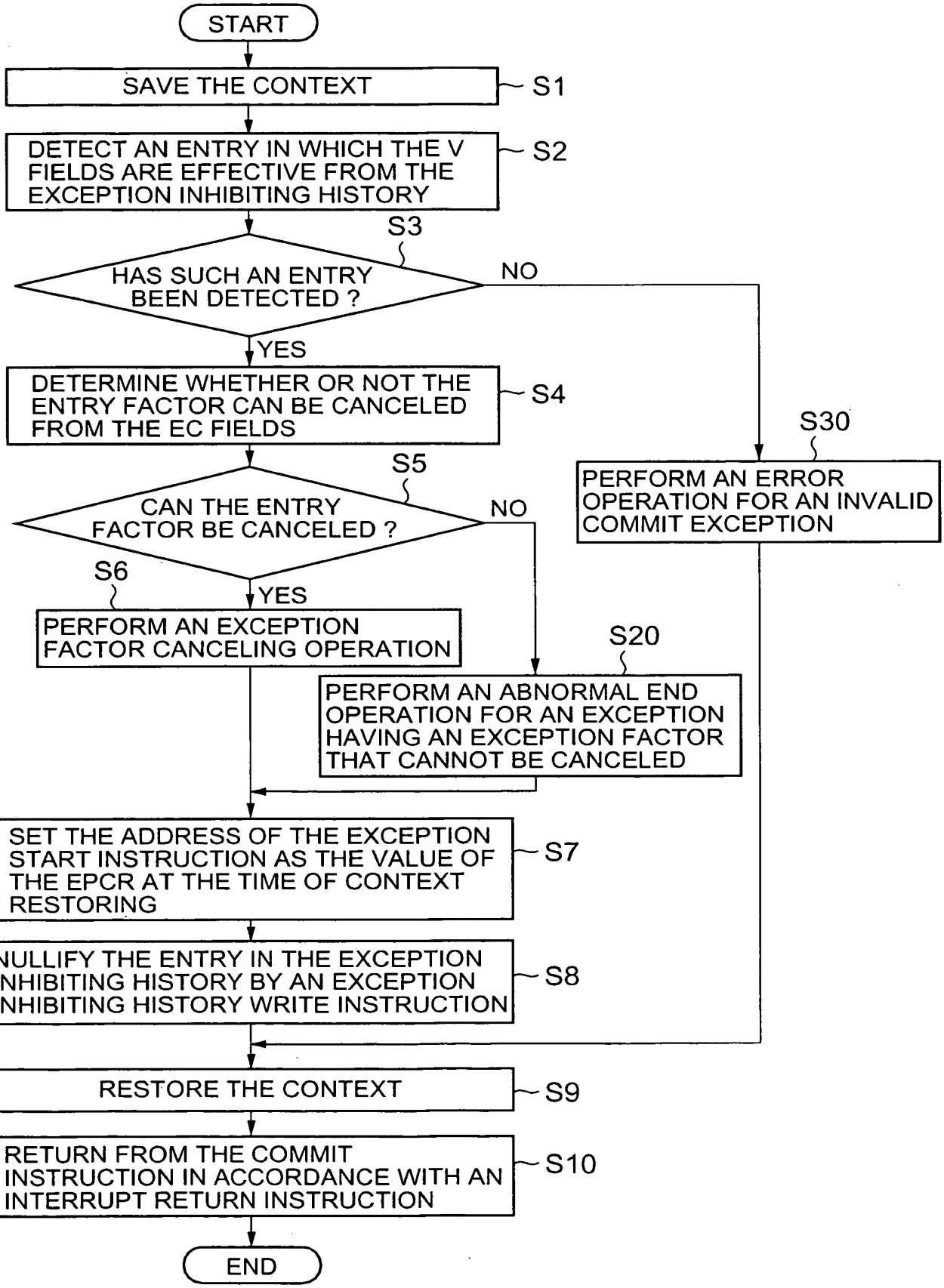

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FIG.50

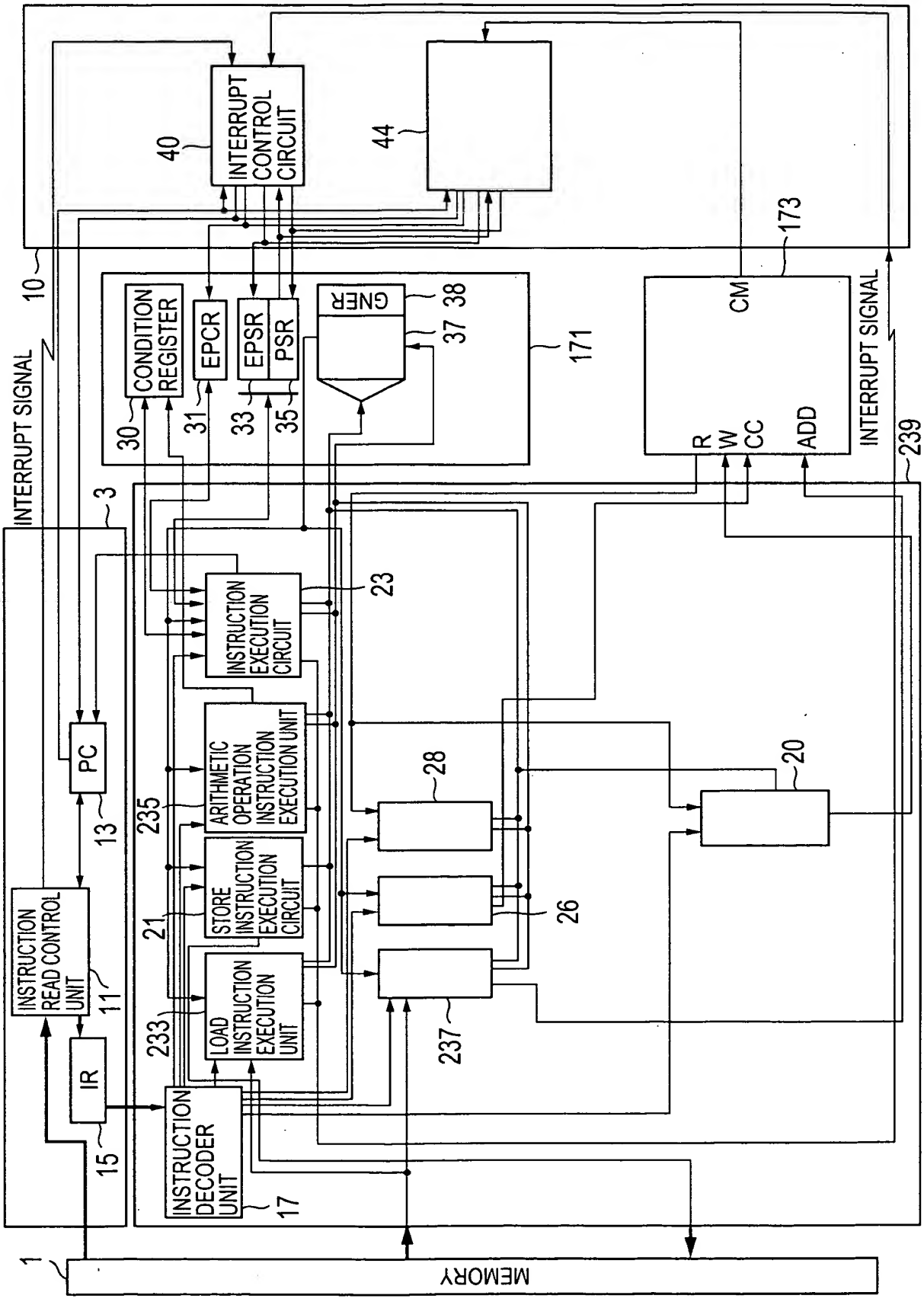
MEMORY
1
INSTRUCTION SIGNAL
10
INTERRUPT CONTROL CIRCUIT
40
44
CONDITION REGISTER
30
EPCR
31
EPSR
33
PSR
35
GNFR
37 38
171
CM
173
R
W
CC
ADD
INTERRUPT SIGNAL
239
3
INSTRUCTION EXECUTION CIRCUIT
23
ARITHMETIC OPERATION INSTRUCTION EXECUTION UNIT
235
PC
13
STORE INSTRUCTION EXECUTION CIRCUIT
21
LOAD INSTRUCTION EXECUTION UNIT
233
INSTRUCTION READ CONTROL UNIT
11
IR
15
INSTRUCTION DECODER UNIT
17
28
26
237
20

FIG. 51

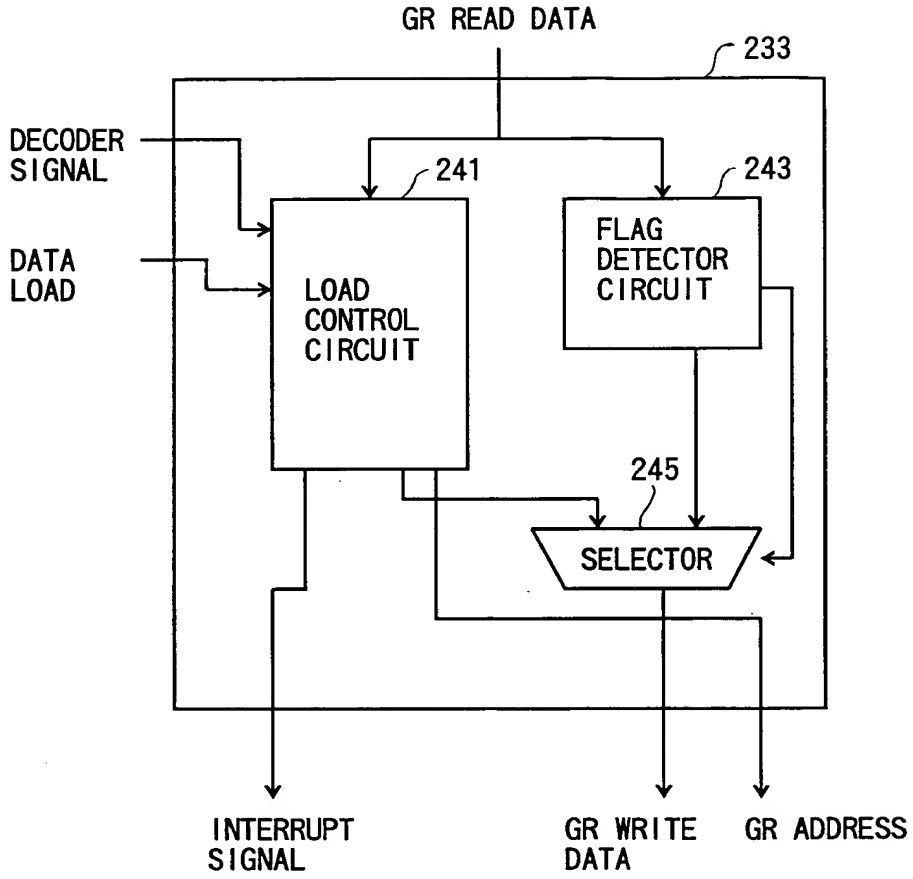
GR READ DATA
233
DECODER SIGNAL
241
243
DATA LOAD
LOAD CONTROL CIRCUIT
FLAG DETECTOR CIRCUIT
245
SELECTOR
INTERRUPT SIGNAL
GR WRITE DATA
GR ADDRESS

FIG. 52

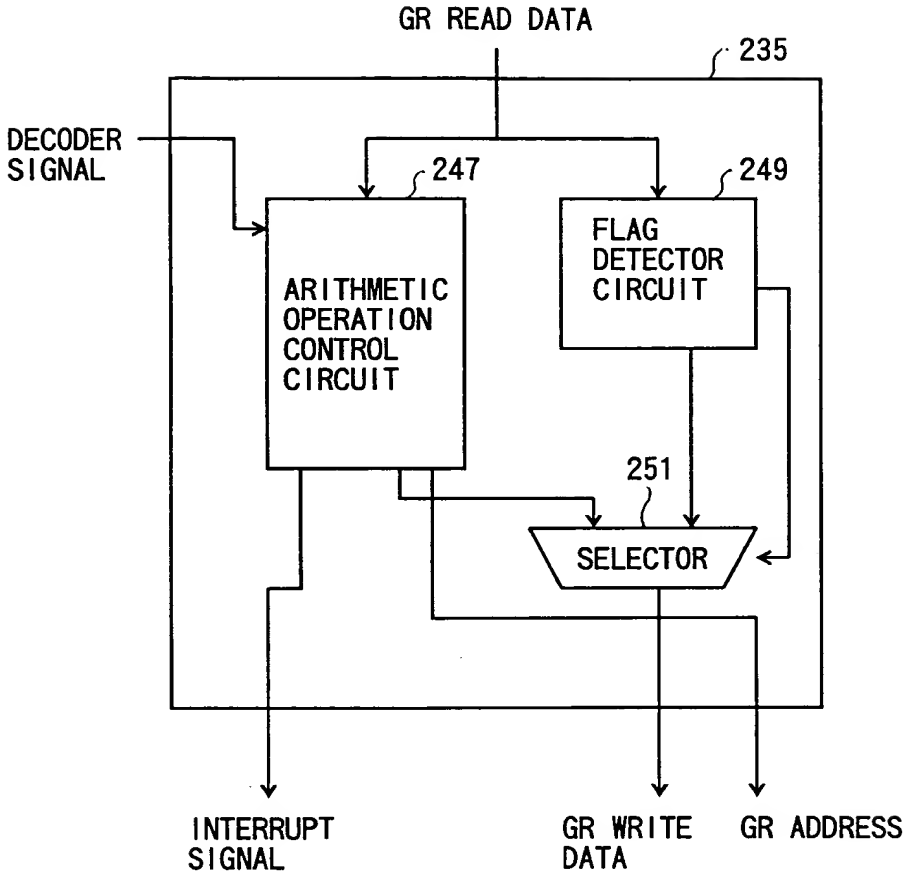
GR READ DATA
235
DECODER SIGNAL
247
249
ARITHMETIC OPERATION CONTROL CIRCUIT
FLAG DETECTOR CIRCUIT
251
SELECTOR
INTERRUPT SIGNAL
GR WRITE DATA
GR ADDRESS

FIG. 53

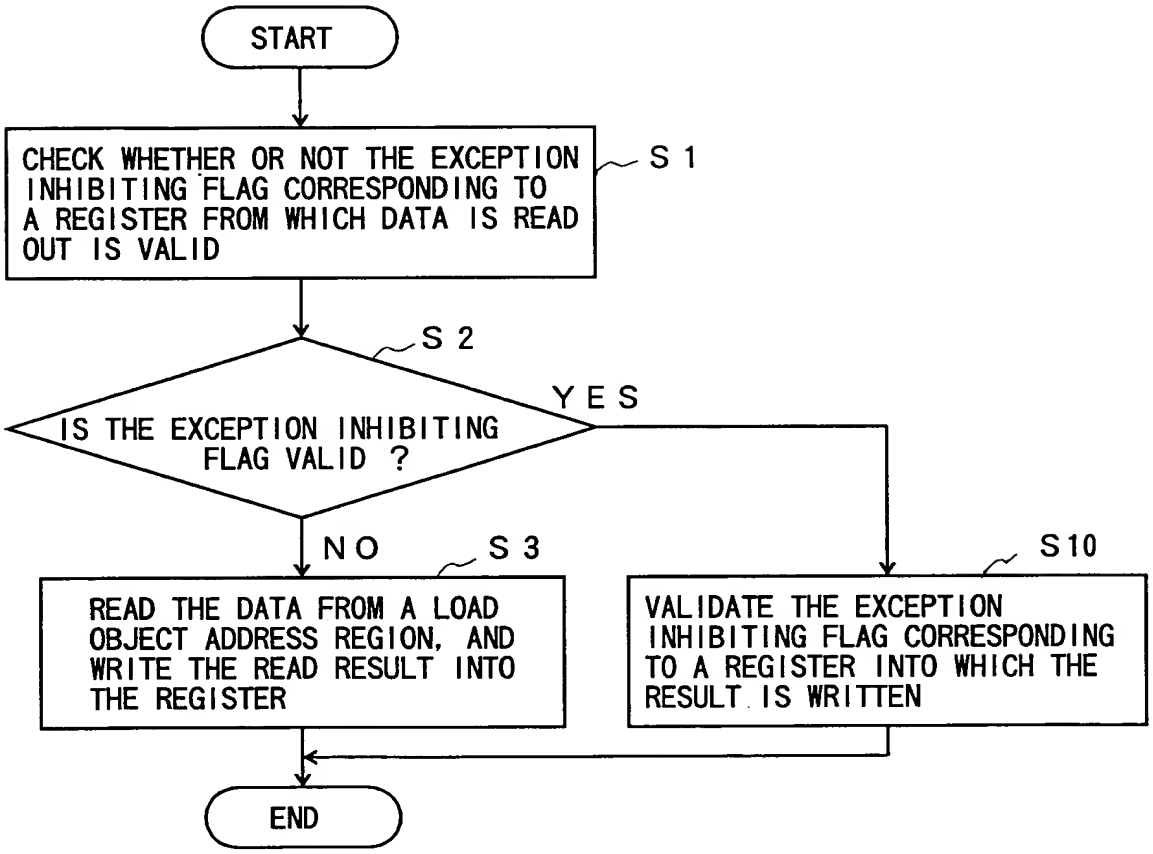
START
CHECK WHETHER OR NOT THE EXCEPTION INHIBITING FLAG CORRESPONDING TO A REGISTER FROM WHICH DATA IS READ OUT IS VALID
S 1
S 2
IS THE EXCEPTION INHIBITING FLAG VALID ?
YES
NO
S 3
READ THE DATA FROM A LOAD OBJECT ADDRESS REGION, AND WRITE THE READ RESULT INTO THE REGISTER
S10
VALIDATE THE EXCEPTION INHIBITING FLAG CORRESPONDING TO A REGISTER INTO WHICH THE RESULT IS WRITTEN
END

FIG. 54

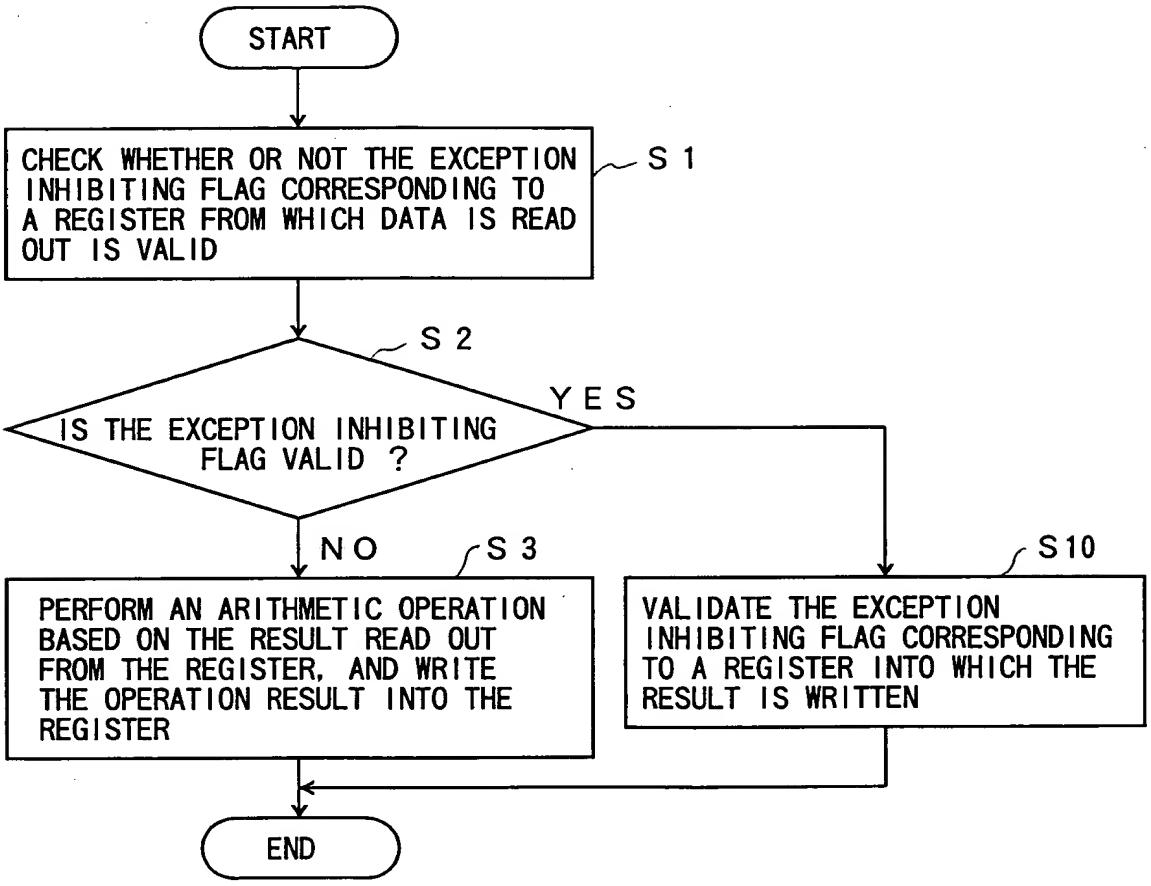

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FIG.55

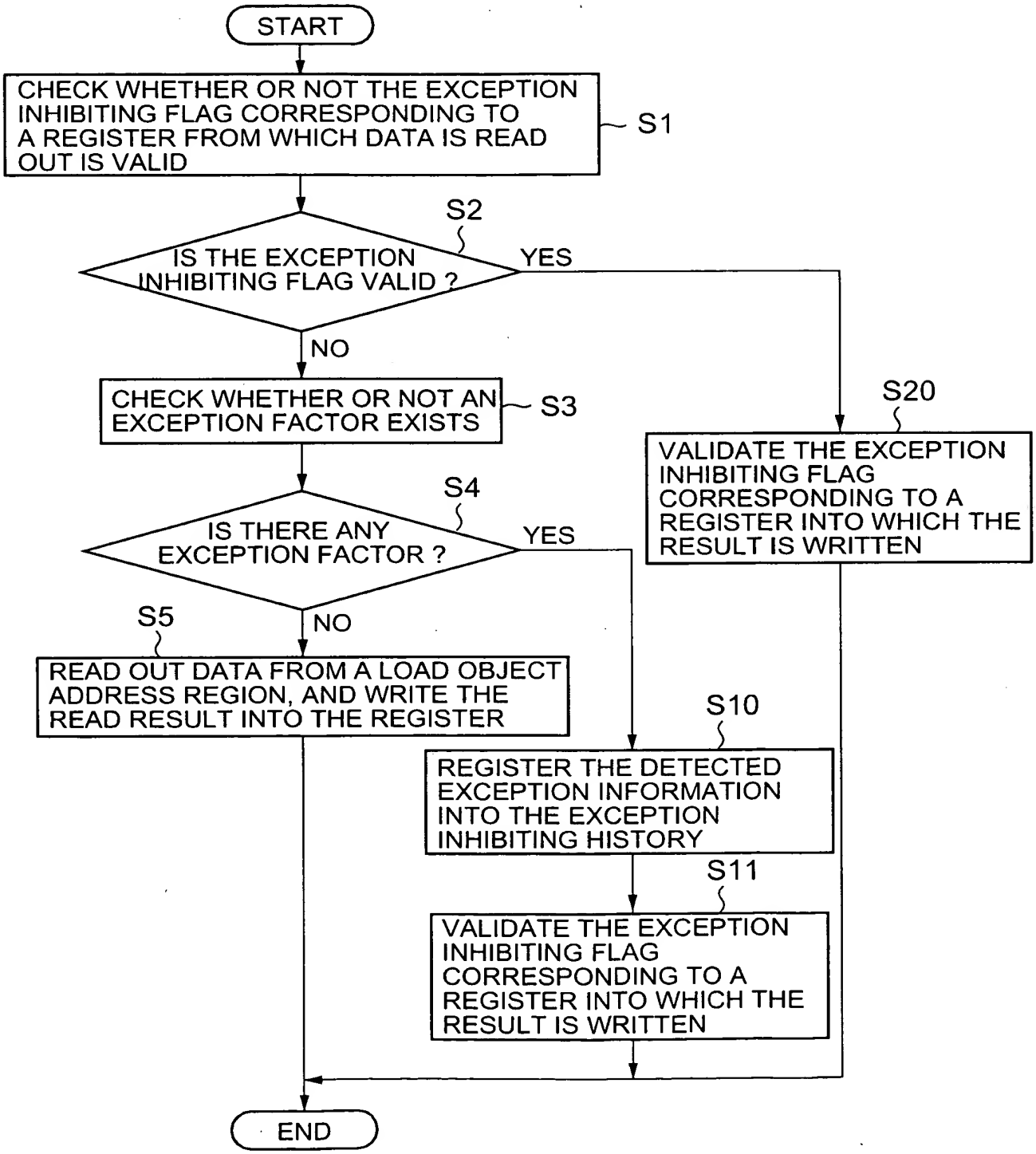

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FIG.56

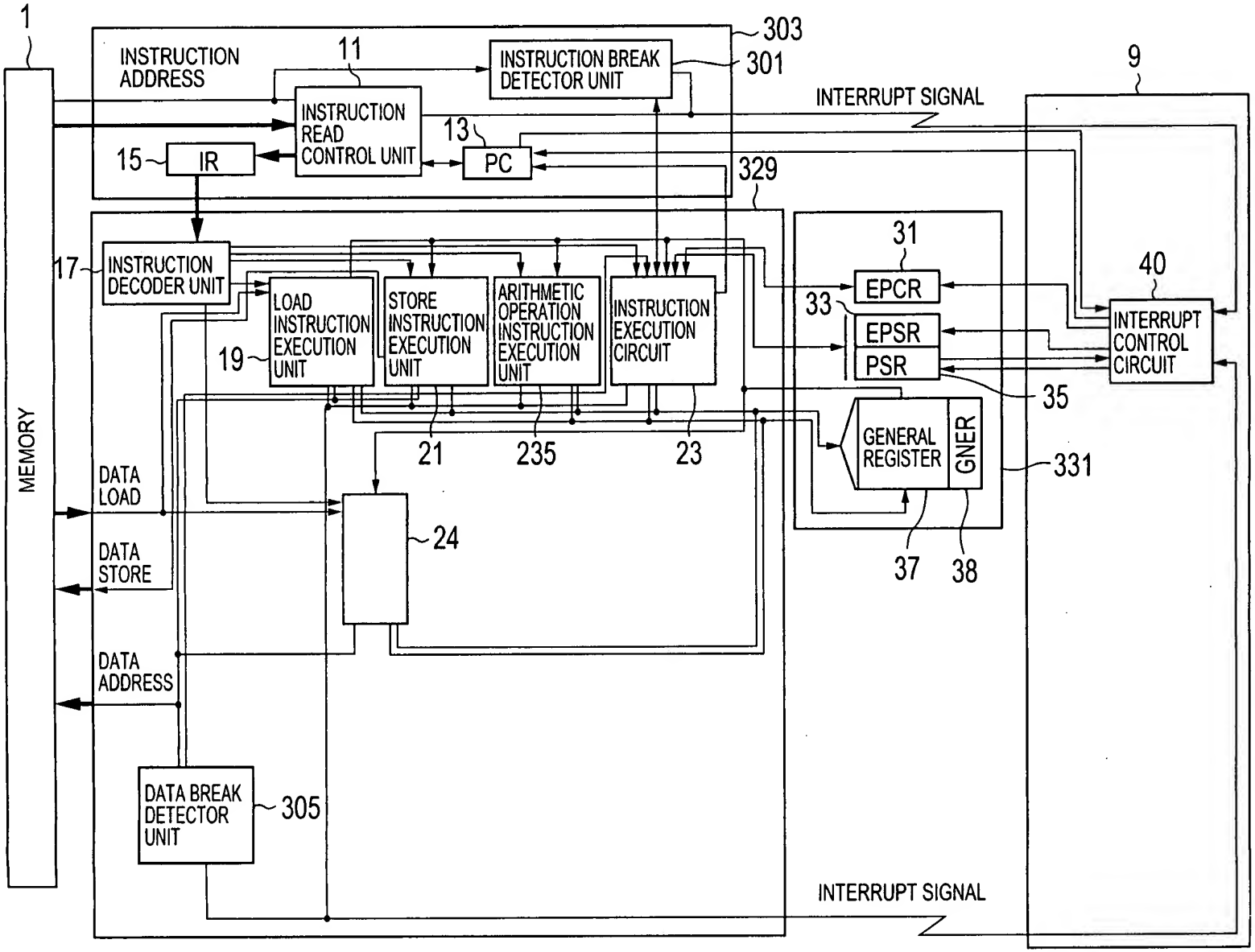
1
MEMORY
INSTRUCTION ADDRESS
11
INSTRUCTION BREAK DETECTOR UNIT
303
301
INSTRUCTION READ CONTROL UNIT
13
PC
15
IR
329
INTERRUPT SIGNAL
9
17
INSTRUCTION DECODER UNIT
LOAD INSTRUCTION EXECUTION UNIT
19
STORE INSTRUCTION EXECUTION UNIT
ARITHMETIC OPERATION INSTRUCTION EXECUTION UNIT
INSTRUCTION EXECUTION CIRCUIT
21
235
23
31
EPCR
33
EPSR
PSR
35
40
INTERRUPT CONTROL CIRCUIT
GENERAL REGISTER
GNER
331
37
38
DATA LOAD
DATA STORE
DATA ADDRESS
24
DATA BREAK DETECTOR UNIT
305
INTERRUPT SIGNAL

FIG.57

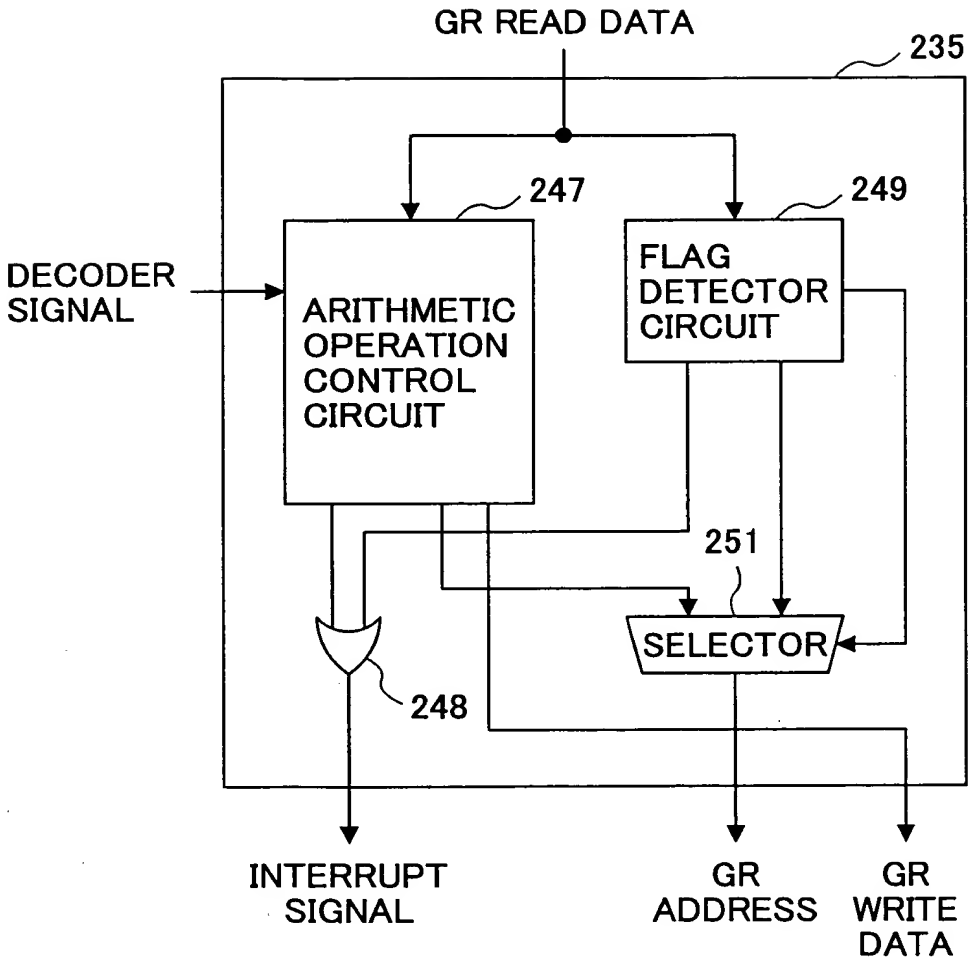
GR READ DATA
235
247
249
DECODER SIGNAL
ARITHMETIC OPERATION CONTROL CIRCUIT
FLAG DETECTOR CIRCUIT
251
SELECTOR
248
INTERRUPT SIGNAL
GR ADDRESS
GR WRITE DATA

FIG.58

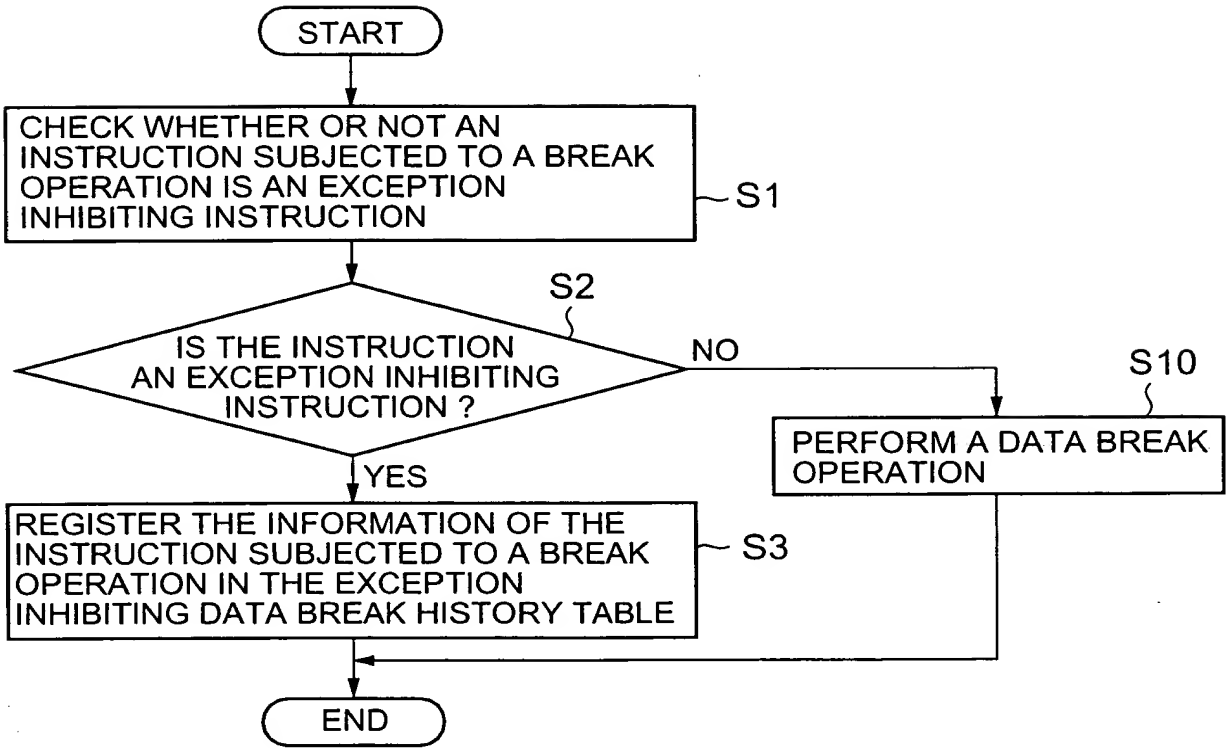

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FIG.59

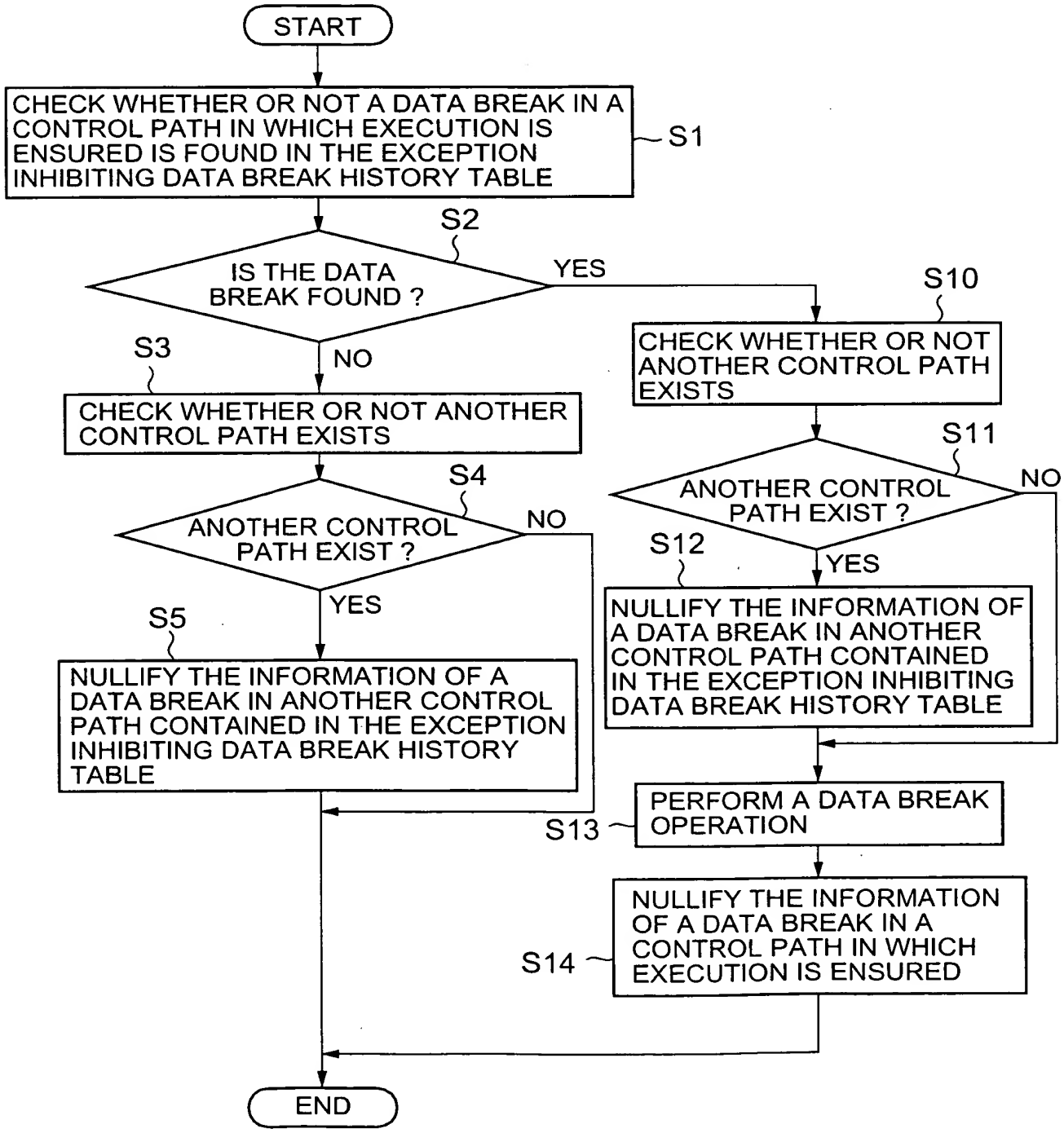

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FIG.60

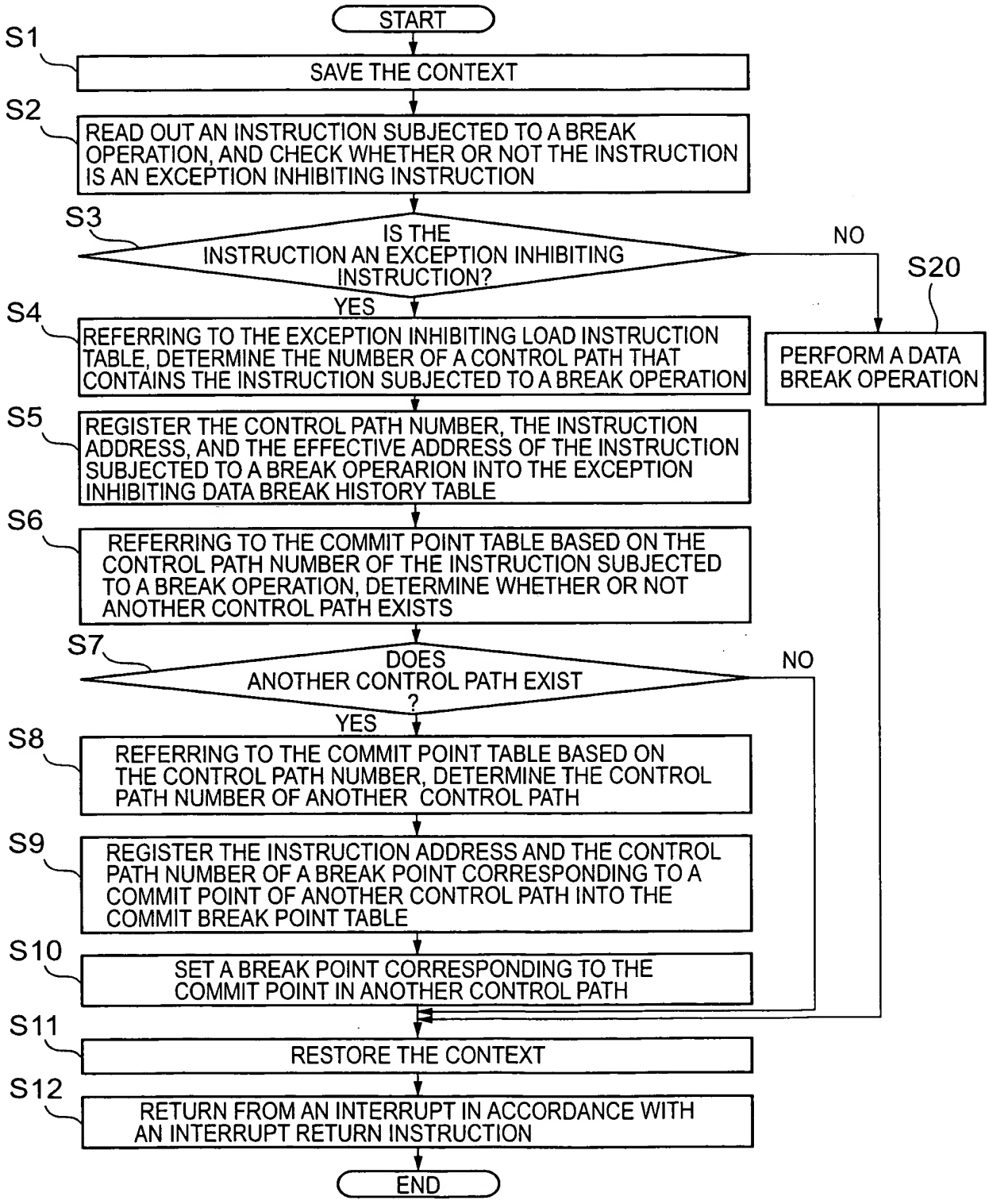

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FIG.61

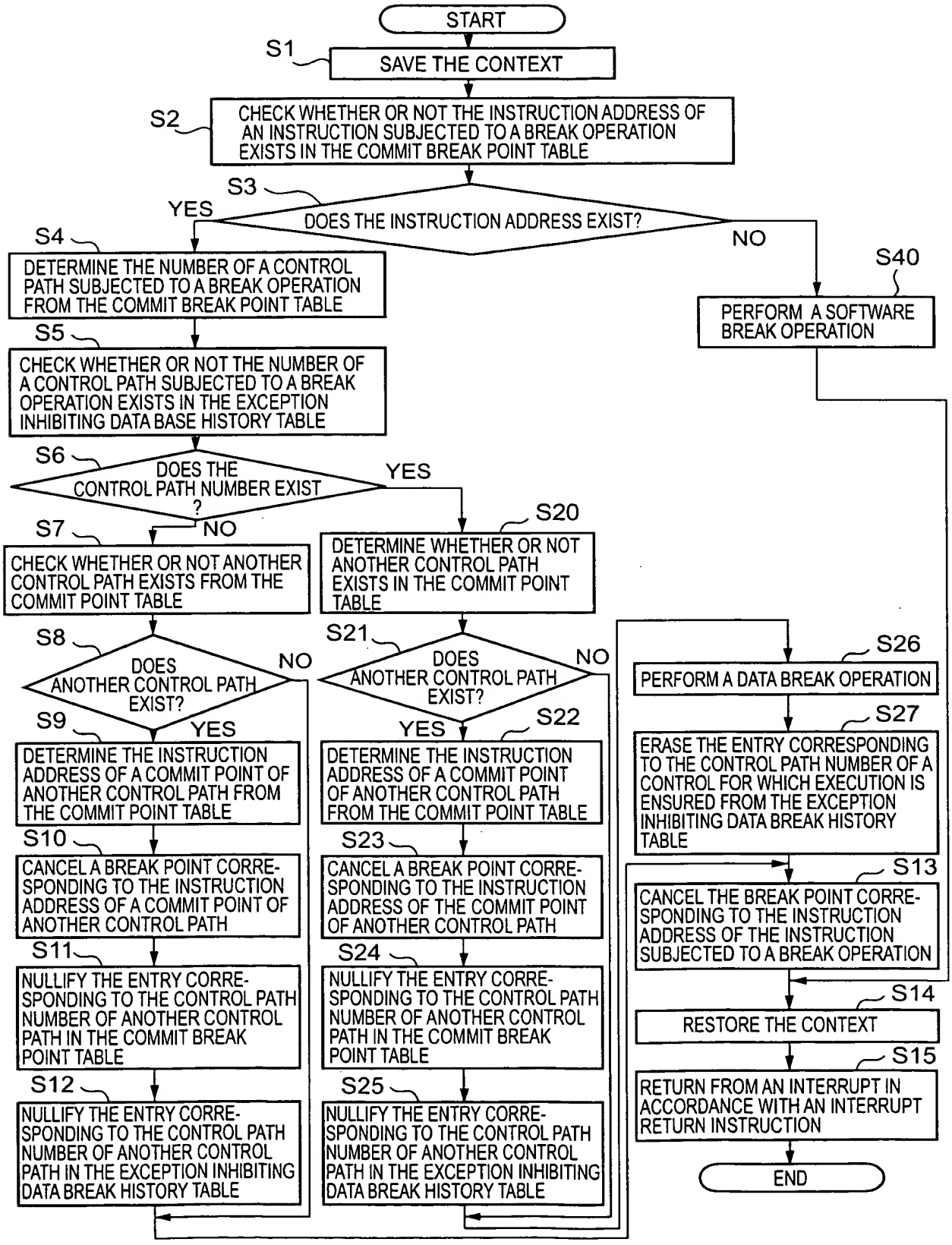
START
S1
SAVE THE CONTEXT
S2
CHECK WHETHER OR NOT THE INSTRUCTION ADDRESS OF AN INSTRUCTION SUBJECTED TO A BREAK OPERATION EXISTS IN THE COMMIT BREAK POINT TABLE
S3
DOES THE INSTRUCTION ADDRESS EXIST?
YES
NO
S4
DETERMINE THE NUMBER OF A CONTROL PATH SUBJECTED TO A BREAK OPERATION FROM THE COMMIT BREAK POINT TABLE
S40
PERFORM A SOFTWARE BREAK OPERATION
S5
CHECK WHETHER OR NOT THE NUMBER OF A CONTROL PATH SUBJECTED TO A BREAK OPERATION EXISTS IN THE EXCEPTION INHIBITING DATA BASE HISTORY TABLE
S6
DOES THE CONTROL PATH NUMBER EXIST ?
YES
NO
S7
CHECK WHETHER OR NOT ANOTHER CONTROL PATH EXISTS FROM THE COMMIT POINT TABLE
S20
DETERMINE WHETHER OR NOT ANOTHER CONTROL PATH EXISTS IN THE COMMIT POINT TABLE
S8
DOES ANOTHER CONTROL PATH EXIST?
NO
YES
S9
DETERMINE THE INSTRUCTION ADDRESS OF A COMMIT POINT OF ANOTHER CONTROL PATH FROM THE COMMIT POINT TABLE
S10
CANCEL A BREAK POINT CORRESPONDING TO THE INSTRUCTION ADDRESS OF A COMMIT POINT OF ANOTHER CONTROL PATH
S11
NULLIFY THE ENTRY CORRESPONDING TO THE CONTROL PATH NUMBER OF ANOTHER CONTROL PATH IN THE COMMIT BREAK POINT TABLE
S12
NULLIFY THE ENTRY CORRESPONDING TO THE CONTROL PATH NUMBER OF ANOTHER CONTROL PATH IN THE EXCEPTION INHIBITING DATA BREAK HISTORY TABLE
S21
DOES ANOTHER CONTROL PATH EXIST?
NO
YES
S22
DETERMINE THE INSTRUCTION ADDRESS OF A COMMIT POINT OF ANOTHER CONTROL PATH FROM THE COMMIT POINT TABLE
S23
CANCEL A BREAK POINT CORRESPONDING TO THE INSTRUCTION ADDRESS OF THE COMMIT POINT OF ANOTHER CONTROL PATH
S24
NULLIFY THE ENTRY CORRESPONDING TO THE CONTROL PATH NUMBER OF ANOTHER CONTROL PATH IN THE COMMIT BREAK POINT TABLE
S25
NULLIFY THE ENTRY CORRESPONDING TO THE CONTROL PATH NUMBER OF ANOTHER CONTROL PATH IN THE EXCEPTION INHIBITING DATA BREAK HISTORY TABLE
S26
PERFORM A DATA BREAK OPERATION
S27
ERASE THE ENTRY CORRESPONDING TO THE CONTROL PATH NUMBER OF A CONTROL FOR WHICH EXECUTION IS ENSURED FROM THE EXCEPTION INHIBITING DATA BREAK HISTORY TABLE
S13
CANCEL THE BREAK POINT CORRESPONDING TO THE INSTRUCTION ADDRESS OF THE INSTRUCTION SUBJECTED TO A BREAK OPERATION
S14
RESTORE THE CONTEXT
S15
RETURN FROM AN INTERRUPT IN ACCORDANCE WITH AN INTERRUPT RETURN INSTRUCTION
END

FIG.62

INSTRUCTION ADDRESS	PATH IDENTIFICATION NUMBER
a0	p0
a1	p1
:	:
:	:
ai	pi

FIG.63

PATH IDENTIFICATION NUMBER	INSTRUCTION ADDRESS	ANOTHER PATH IDENTIFICATION NUMBER
p0	b0	sp0
p1	b1	sp1
:	:	:
:	:	:
pj	bj	spj

FIG.64

INSTRUCTION ADDRESS	PATH IDENTIFICATION NUMBER
b0	p0
b1	p1
:	:
:	:
bk	pk

FIG.65

PATH IDENTIFICATION NUMBER	INSTRUCTION ADDRESS	EFFECTIVE ADDRESS
p0	c0	ec0
p1	c1	ec1
:	:	:
:	:	:
pl	cl	ecl

FIG.66

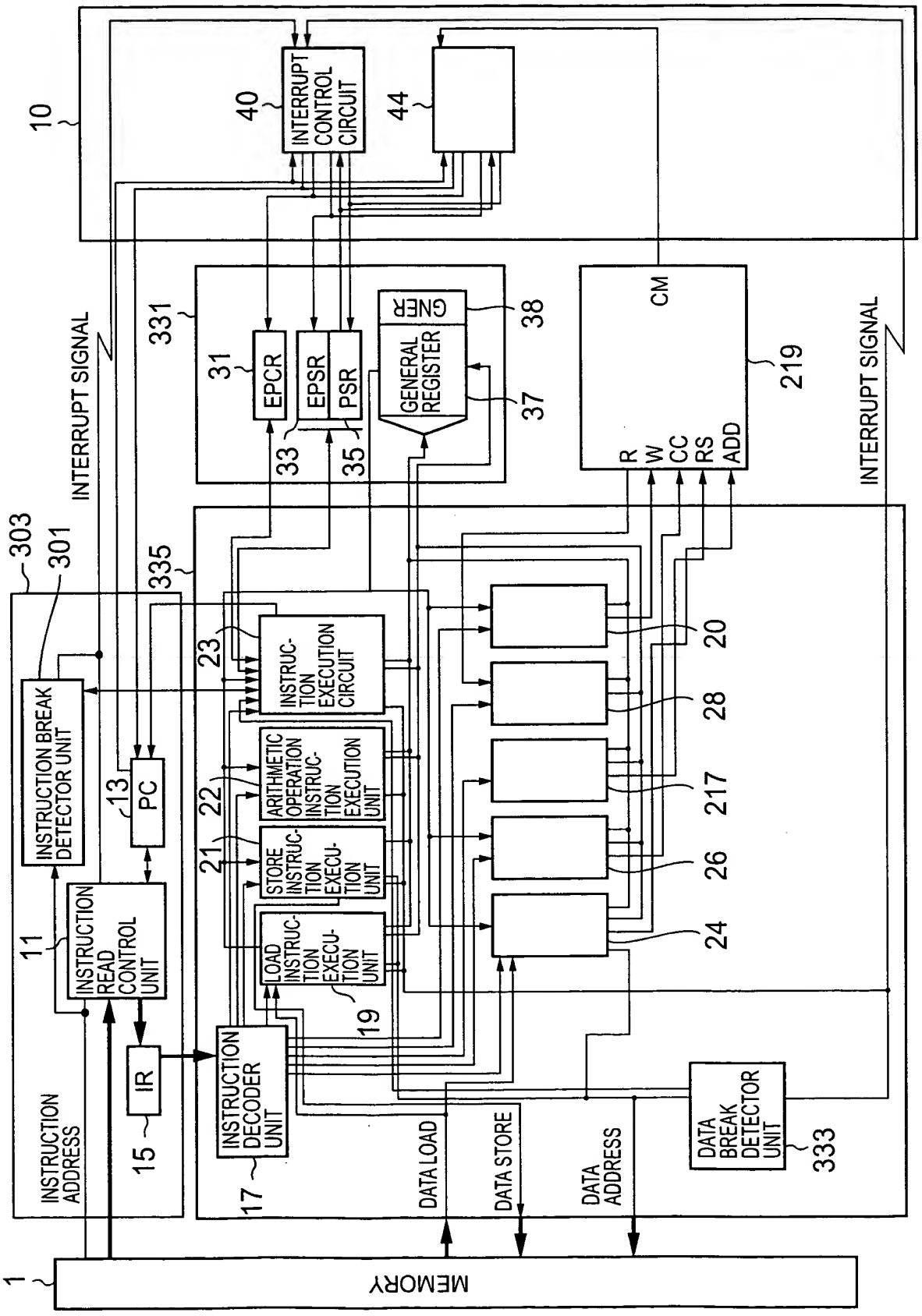
10
40
INTERRUPT CONTROL CIRCUIT
44
INTERRUPT SIGNAL
331
31
EPCR
EPSR
PSR
33
35
GENERAL REGISTER
GNER
38
37
CM
R
W
CC
RS
ADD
219
INTERRUPT SIGNAL
303
301
335
INSTRUCTION BREAK DETECTOR UNIT
INSTRUC-TION EXECUTION CIRCUIT
23
20
13
PC
ARITHMETIC OPERATION INSTRUC-TION EXECUTION UNIT
22
28
21
STORE INSTRUC-TION EXECU-TION UNIT
217
26
LOAD INSTRUC-TION EXECU-TION UNIT
24
19
11
INSTRUCTION READ CONTROL UNIT
INSTRUCTION DECODER UNIT
17
IR
15
INSTRUCTION ADDRESS
DATA LOAD
DATA STORE
DATA ADDRESS
DATA BREAK DETECTOR UNIT
333
1
MEMORY

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FIG.67

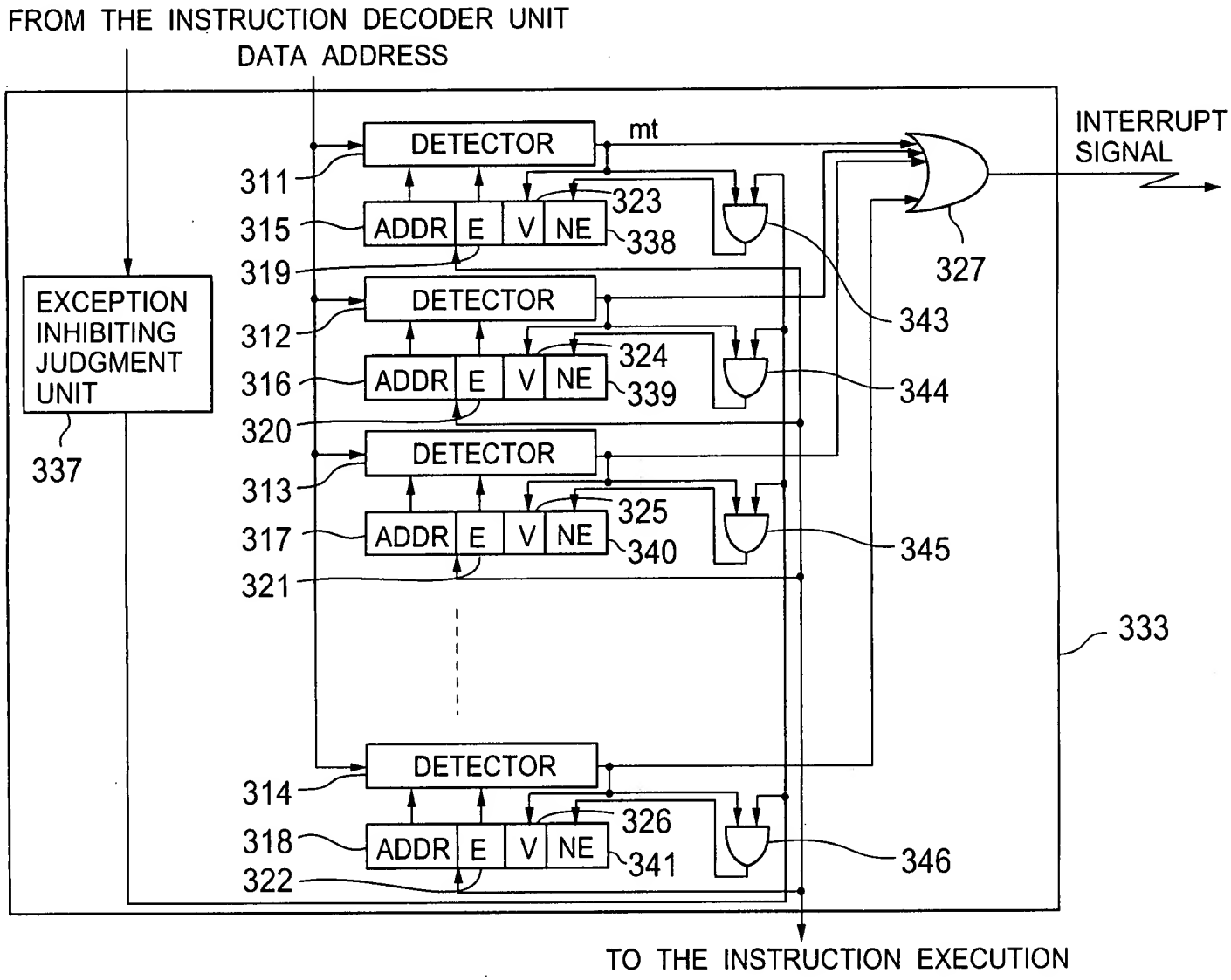

FIG.68

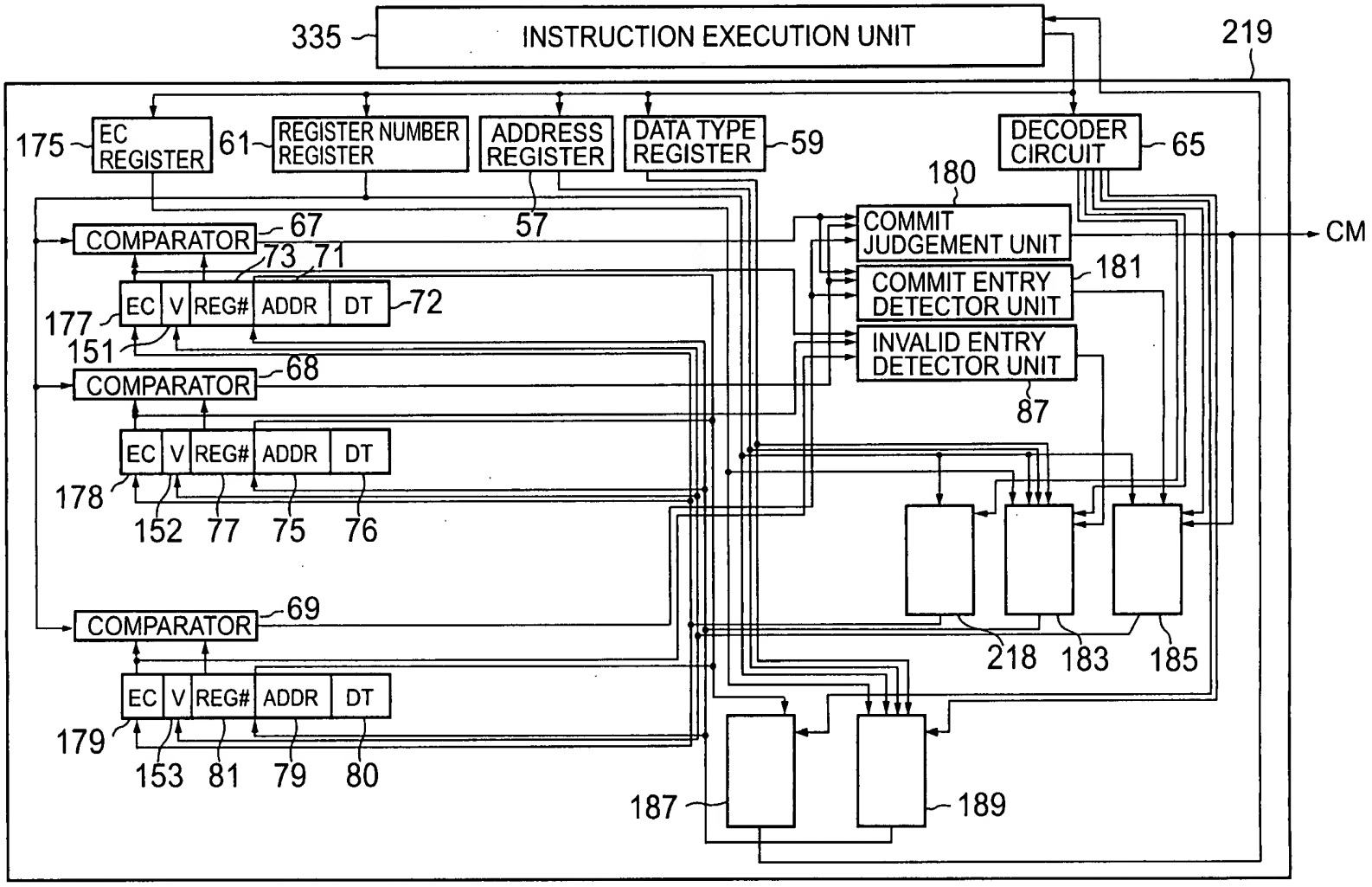
335
INSTRUCTION EXECUTION UNIT
219
175
EC REGISTER
61
REGISTER NUMBER REGISTER
ADDRESS REGISTER
DATA TYPE REGISTER
59
DECODER CIRCUIT
65
180
COMMIT JUDGEMENT UNIT
CM
COMMIT ENTRY DETECTOR UNIT
181
INVALID ENTRY DETECTOR UNIT
87
COMPARATOR
67
57
73
71
EC
V
REG#
ADDR
DT
72
177
151
COMPARATOR
68
178
152
77
75
76
COMPARATOR
69
179
153
81
79
80
218
183
185
187
189

FIG.69

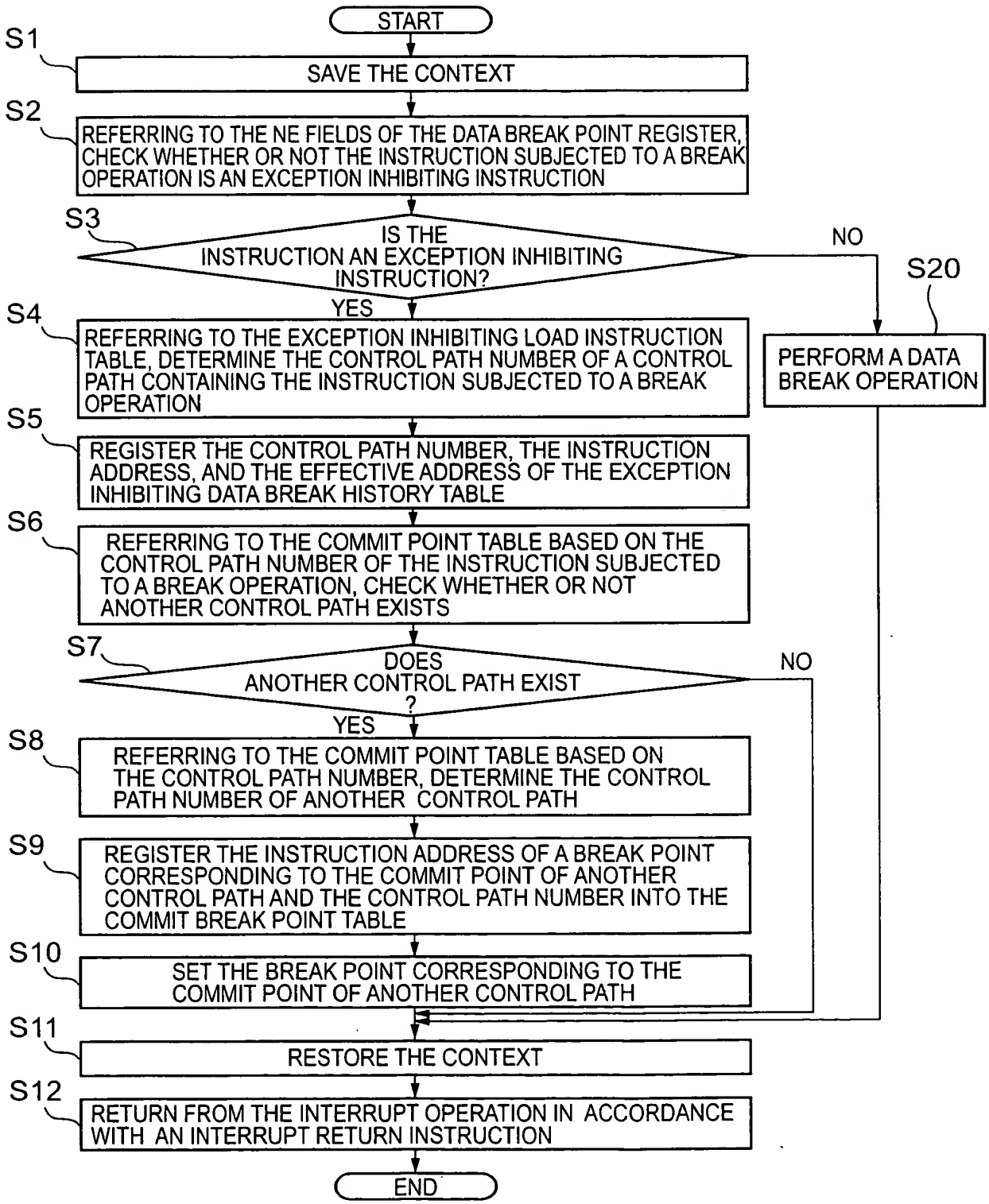

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FIG.70

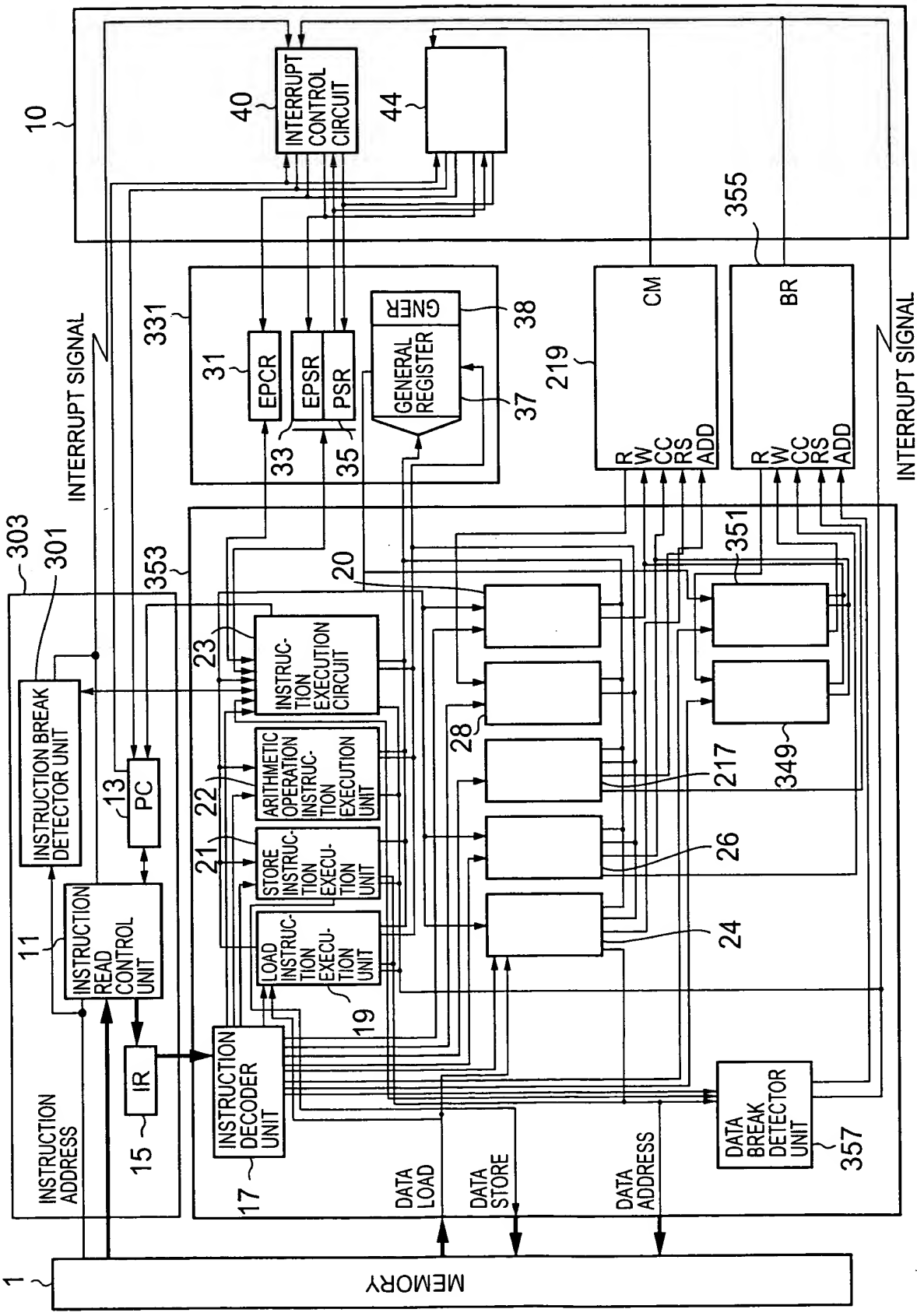
10
40
INTERRUPT CONTROL CIRCUIT
44
355
331
31
EPCR
EPSR
PSR
33
35
GENERAL REGISTER
GNER
38
37
219
CM
BR
R
W
CC
RS
ADD
INTERRUPT SIGNAL
303
301
353
20
351
INSTRUCTION BREAK DETECTOR UNIT
INSTRUC-TION EXECUTION CIRCUIT
23
13
PC
ARITHMETIC OPERATION INSTRUC-TION EXECUTION UNIT
22
28
217
349
21
STORE INSTRUC-TION EXECU-TION UNIT
26
11
INSTRUCTION READ CONTROL UNIT
LOAD INSTRUC-TION EXECU-TION UNIT
19
24
INSTRUCTION ADDRESS
15
IR
INSTRUCTION DECODER UNIT
17
DATA LOAD
DATA STORE
DATA ADDRESS
DATA BREAK DETECTOR UNIT
357
1
MEMORY

FIG.71

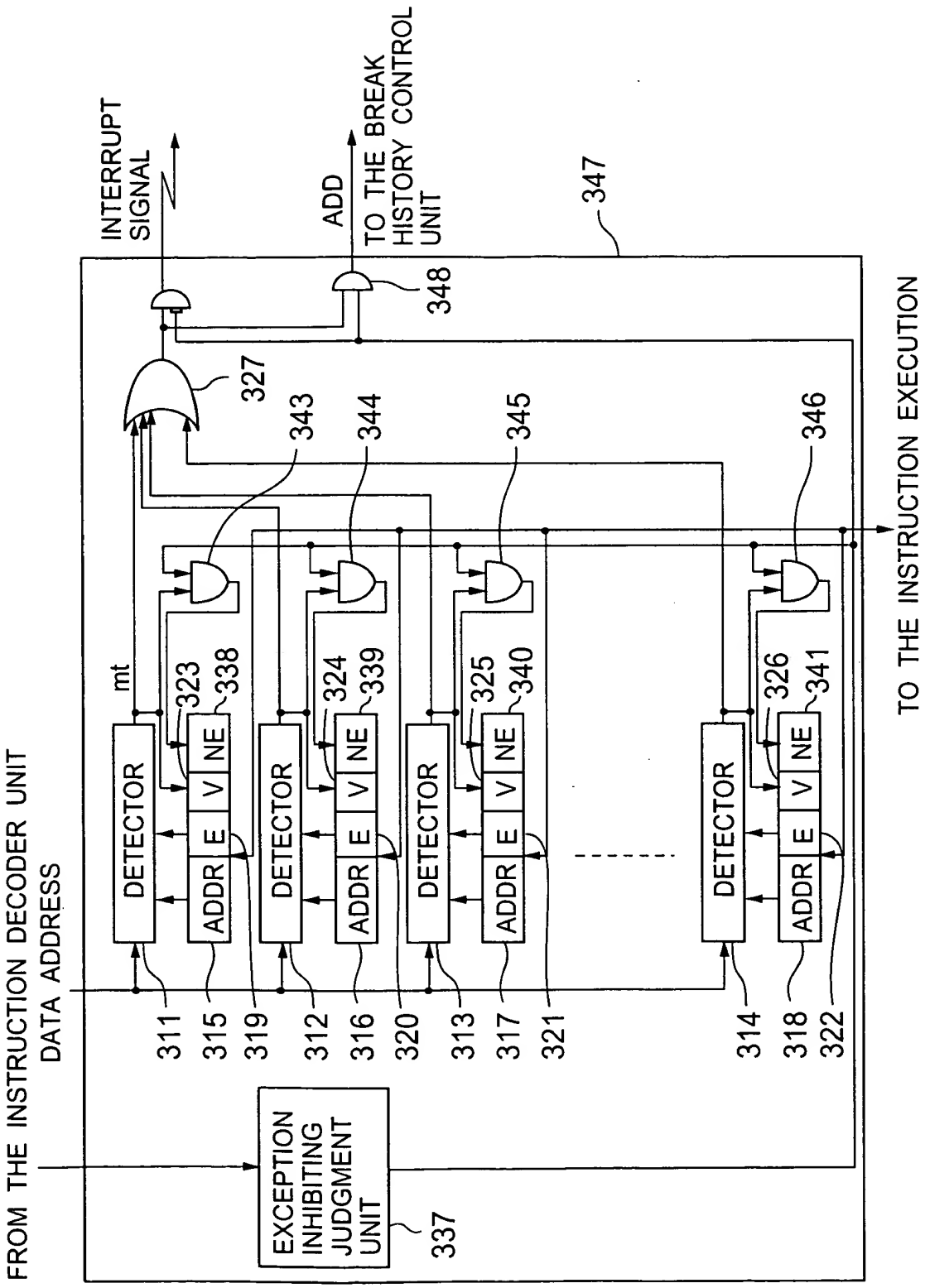
FROM THE INSTRUCTION DECODER UNIT
DATA ADDRESS
INTERRUPT SIGNAL
ADD
TO THE BREAK HISTORY CONTROL UNIT
TO THE INSTRUCTION EXECUTION
EXCEPTION INHIBITING JUDGMENT UNIT
337
DETECTOR
ADDR
E
V
NE
mt
311
312
313
314
315
316
317
318
319
320
321
322
323
324
325
326
327
338
339
340
341
343
344
345
346
347
348

FIG.72

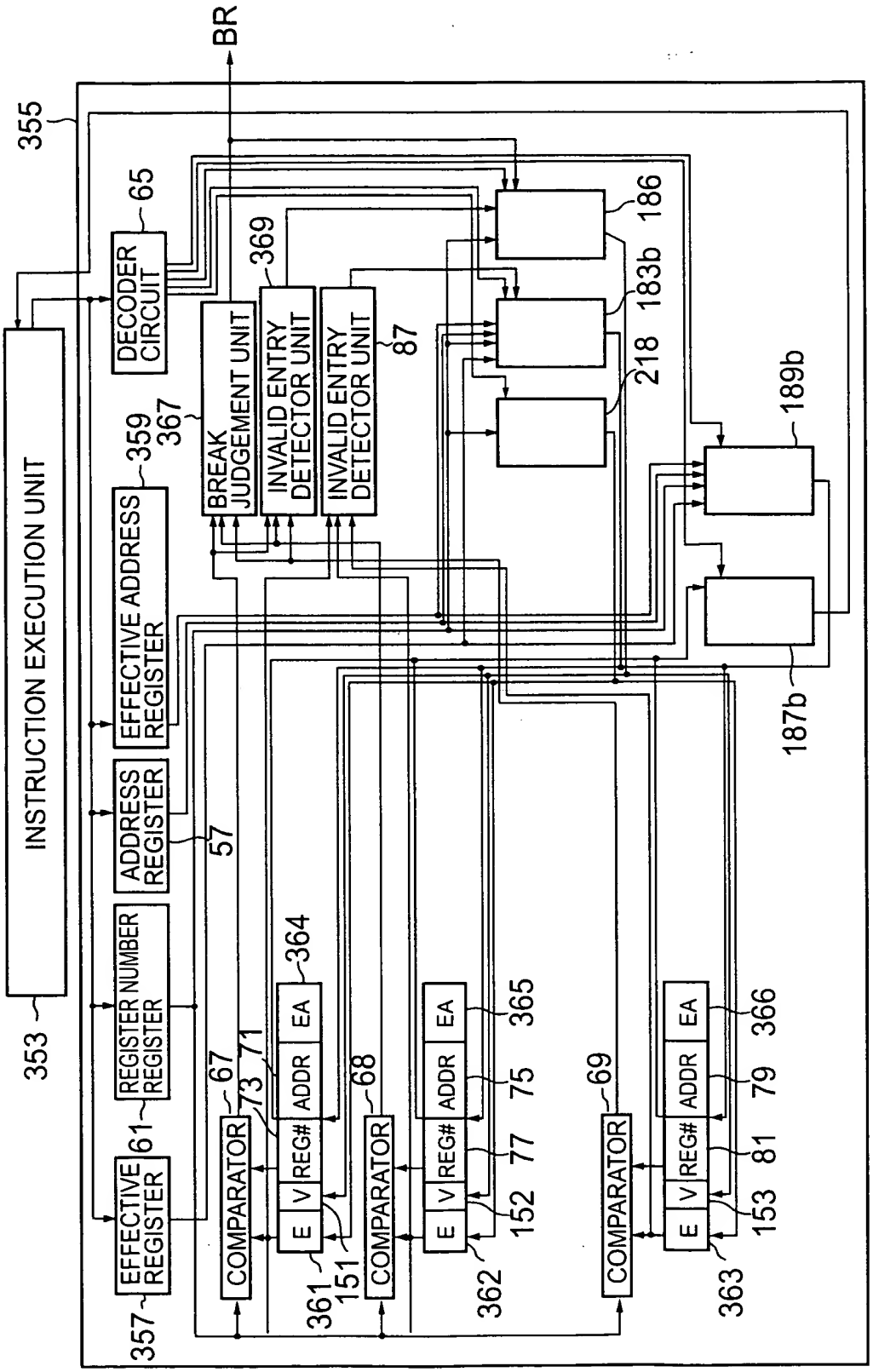
BR
355
INSTRUCTION EXECUTION UNIT
353
DECODER CIRCUIT
65
EFFECTIVE ADDRESS REGISTER
359
BREAK JUDGEMENT UNIT
367
INVALID ENTRY DETECTOR UNIT
369
INVALID ENTRY DETECTOR UNIT
87
ADDRESS REGISTER
57
REGISTER NUMBER REGISTER
61
EFFECTIVE REGISTER
357
COMPARATOR
67
COMPARATOR
68
COMPARATOR
69
E
V
REG#
ADDR
EA
364
365
366
361
362
363
151
152
153
71
73
75
77
79
81
186
183b
218
189b
187b

FIG.73

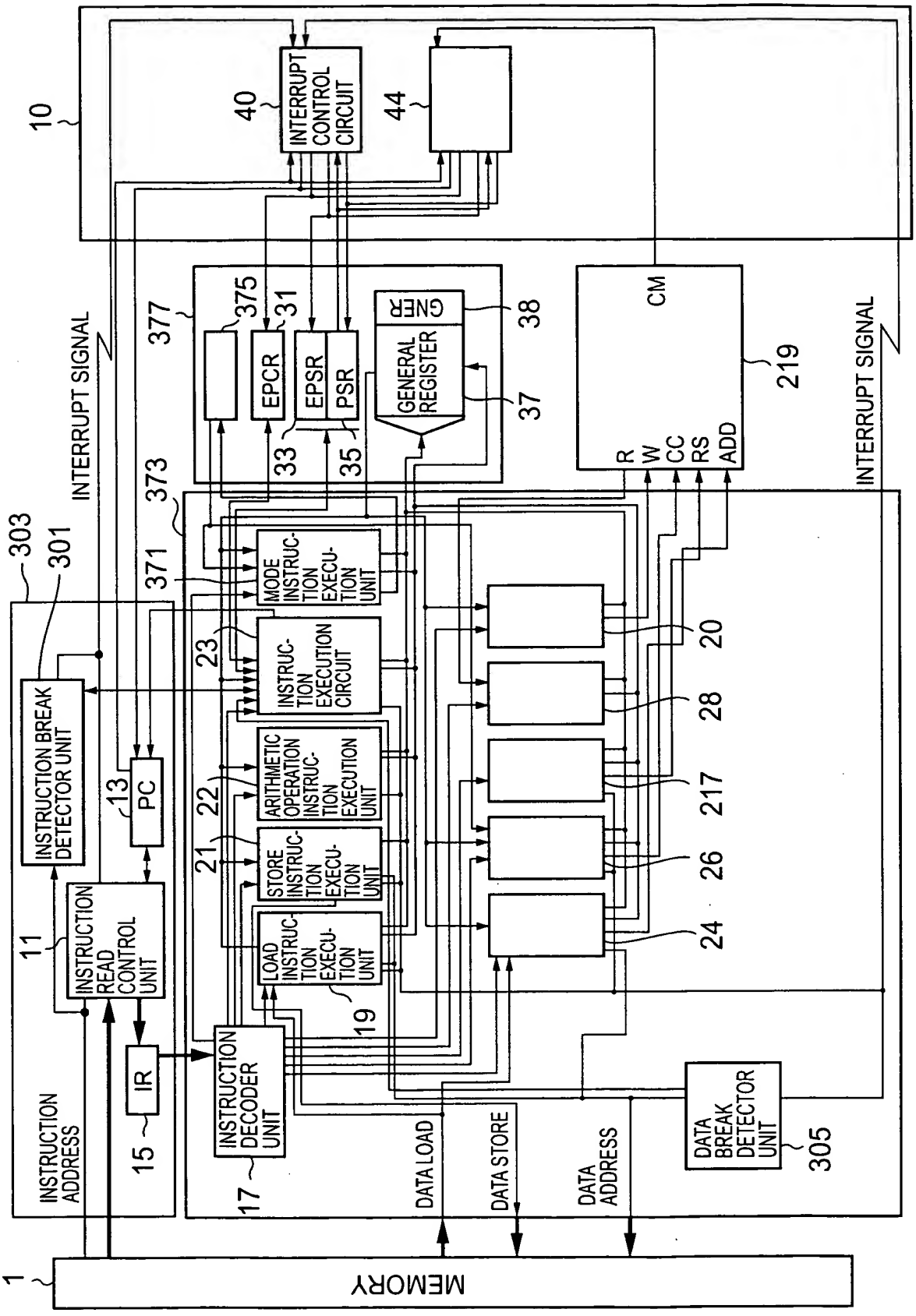
10
40
INTERRUPT CONTROL CIRCUIT
44
INTERRUPT SIGNAL
377
375
31
EPCR
EPSR
PSR
GENERAL REGISTER
GNER
38
37
33
35
CM
R
W
CC
RS
ADD
219
INTERRUPT SIGNAL
303
301
371
373
MODE INSTRUCTION EXECUTION UNIT
INSTRUCTION EXECUTION CIRCUIT
ARITHMETIC OPERATION INSTRUCTION EXECUTION UNIT
STORE INSTRUCTION EXECUTION UNIT
LOAD INSTRUCTION EXECUTION UNIT
23
22
21
19
20
28
217
26
24
INSTRUCTION BREAK DETECTOR UNIT
PC
13
11
INSTRUCTION READ CONTROL UNIT
IR
15
INSTRUCTION DECODER UNIT
17
INSTRUCTION ADDRESS
DATA LOAD
DATA STORE
DATA ADDRESS
DATA BREAK DETECTOR UNIT
305
1
MEMORY

FIG.74

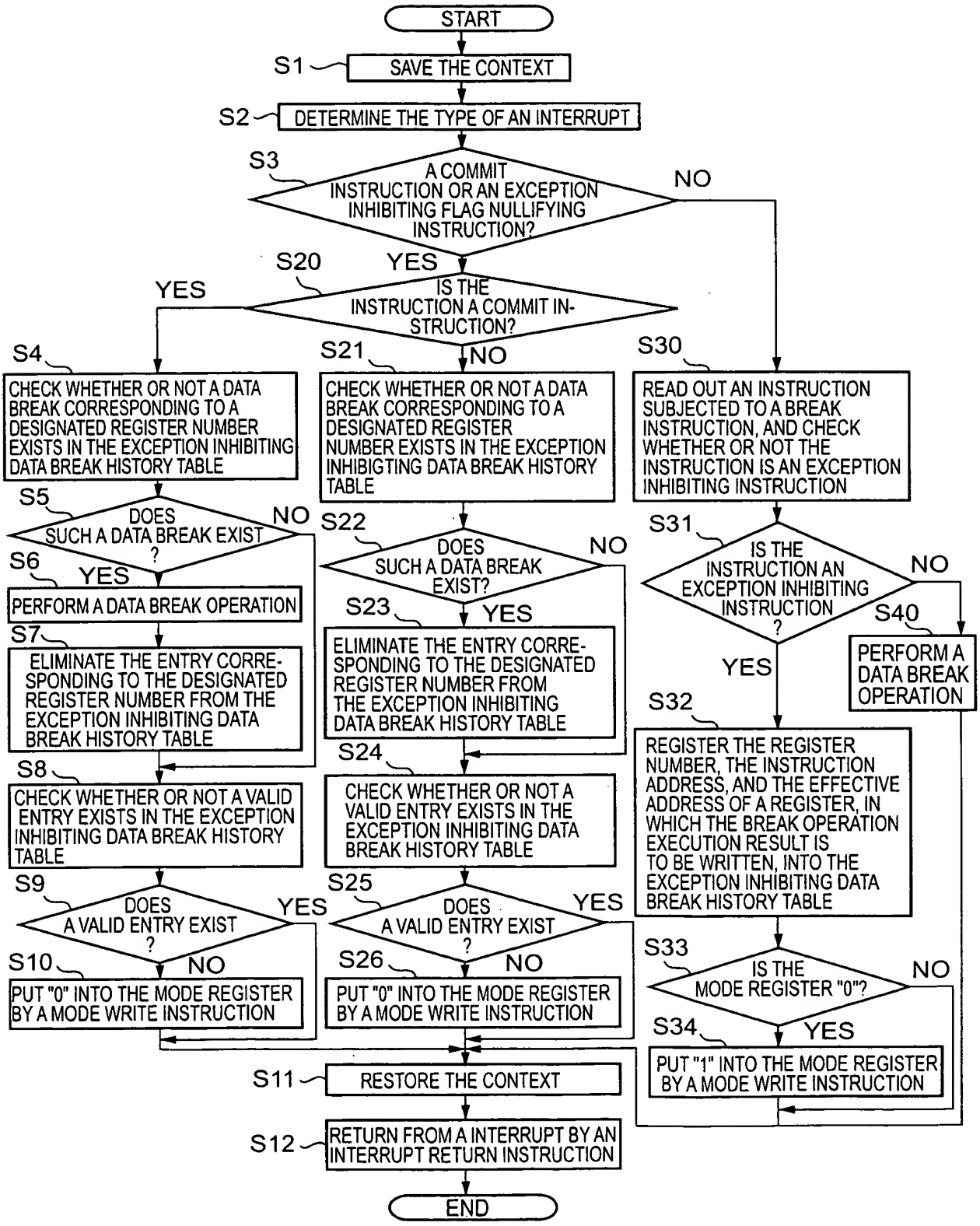
START
S1
SAVE THE CONTEXT
S2
DETERMINE THE TYPE OF AN INTERRUPT
S3
A COMMIT INSTRUCTION OR AN EXCEPTION INHIBITING FLAG NULLIFYING INSTRUCTION?
NO
YES
S20
IS THE INSTRUCTION A COMMIT INSTRUCTION?
YES
NO
S4
CHECK WHETHER OR NOT A DATA BREAK CORRESPONDING TO A DESIGNATED REGISTER NUMBER EXISTS IN THE EXCEPTION INHIBITING DATA BREAK HISTORY TABLE
S21
CHECK WHETHER OR NOT A DATA BREAK CORRESPONDING TO A DESIGNATED REGISTER NUMBER EXISTS IN THE EXCEPTION INHIBIGTING DATA BREAK HISTORY TABLE
S30
READ OUT AN INSTRUCTION SUBJECTED TO A BREAK INSTRUCTION, AND CHECK WHETHER OR NOT THE INSTRUCTION IS AN EXCEPTION INHIBITING INSTRUCTION
S5
DOES SUCH A DATA BREAK EXIST ?
NO
YES
S6
PERFORM A DATA BREAK OPERATION
S7
ELIMINATE THE ENTRY CORRESPONDING TO THE DESIGNATED REGISTER NUMBER FROM THE EXCEPTION INHIBITING DATA BREAK HISTORY TABLE
S22
DOES SUCH A DATA BREAK EXIST?
NO
YES
S23
ELIMINATE THE ENTRY CORRESPONDING TO THE DESIGNATED REGISTER NUMBER FROM THE EXCEPTION INHIBITING DATA BREAK HISTORY TABLE
S31
IS THE INSTRUCTION AN EXCEPTION INHIBITING INSTRUCTION ?
NO
YES
S40
PERFORM A DATA BREAK OPERATION
S32
REGISTER THE REGISTER NUMBER, THE INSTRUCTION ADDRESS, AND THE EFFECTIVE ADDRESS OF A REGISTER, IN WHICH THE BREAK OPERATION EXECUTION RESULT IS TO BE WRITTEN, INTO THE EXCEPTION INHIBITING DATA BREAK HISTORY TABLE
S8
CHECK WHETHER OR NOT A VALID ENTRY EXISTS IN THE EXCEPTION INHIBITING DATA BREAK HISTORY TABLE
S24
CHECK WHETHER OR NOT A VALID ENTRY EXISTS IN THE EXCEPTION INHIBITING DATA BREAK HISTORY TABLE
S9
DOES A VALID ENTRY EXIST ?
YES
NO
S25
DOES A VALID ENTRY EXIST ?
YES
NO
S10
PUT "0" INTO THE MODE REGISTER BY A MODE WRITE INSTRUCTION
S26
PUT "0" INTO THE MODE REGISTER BY A MODE WRITE INSTRUCTION
S33
IS THE MODE REGISTER "0"?
NO
YES
S34
PUT "1" INTO THE MODE REGISTER BY A MODE WRITE INSTRUCTION
S11
RESTORE THE CONTEXT
S12
RETURN FROM A INTERRUPT BY AN INTERRUPT RETURN INSTRUCTION
END

FIG.75

REGISTER NUMBER	INSTRUCTION ADDRESS	EFFECTIVE ADDRESS
r0	a0	ea0
r1	a1	ea1
:	:	:
:	:	:
rl	al	eal

EP 0 926 593 A2